Freescale Semiconductor
Data Sheet: Advance Information

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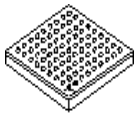
RoHS

MCIMX35

MCIMX35 (i.MX35) Multimedia Applications Processors for Industrial and Consumer Products

Silicon Revision 2.0



Package Information
Plastic package
Case 5284 17 x 17 mm, 0.8 mm Pitch

Ordering Information
See Table 1 on page 3 for ordering information.

1 Introduction

The i.MX353 and the i.MX357 multimedia applications processors represent the next generation of ARM11 products with the right performance and integration to address applications within the industrial and consumer markets for applications such as HMI and display controllers. Unless otherwise specified, the material in this data sheet is applicable to both the i.MX353 and i.MX357 devices and referred to singularly throughout this document as i.MX35 or MCIMX35. The i.MX353 devices do not include a graphics processing unit (GPU). For information on i.MX35 devices for automotive applications, please refer to document number, MCIMX35SR2CEC.

The i.MX35 processor takes advantage of the ARM1136JF-S™ core running at 532 MHz that is boosted by a multi-level cache system and integrated features such as LCD controller, Ethernet, and graphics acceleration for creating rich user interfaces.

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The i.MX35 supports connections to various types of external memories, such as SDRAM, mobile DDR, and DDR2, SLC and MCL NAND Flash, NOR Flash and SRAM. The devices can be connected to a variety of external devices such as USB 2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 Features

It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The MCIMX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY
- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pad port
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)

- Parallel ATA (up to 66 Mbytes)
- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for consumer and industrial applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)
i.MX35 samples	PCIMX357CVM5B	2.0	5284	532 MHz	–40 to 85
i.MX353	MCIMX353CVM5B	2.0	5284	532 MHz	–40 to 85
i.MX353	MCIMX353DVM5B	2.0	5284	532 MHz	–20 to 70
i.MX357	MCIMX357CVM5B	2.0	5284	532 MHz	–40 to 85
i.MX357	MCIMX357DVM5B	2.0	5284	532 MHz	–20 to 70

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1. See application note AN330 for details.

1.3 Block Diagram

Figure 1 is the i.MX35 simplified interface block diagram.

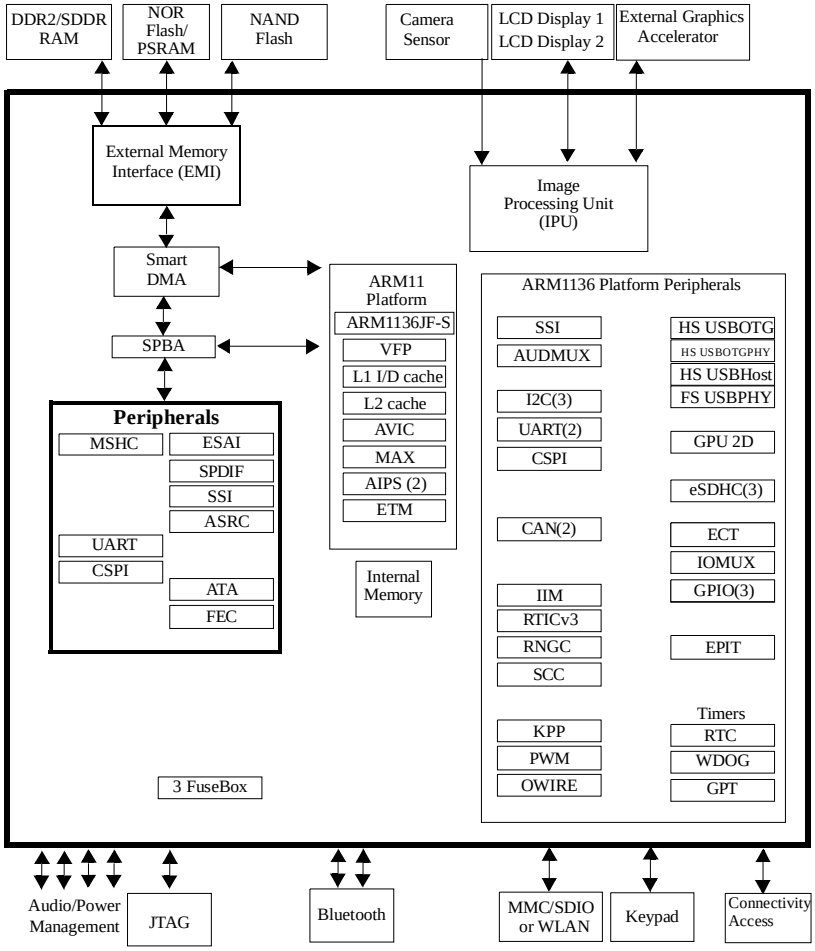


Figure 1. i.MX35 Simplified Interface Block Diagram

2 Functional Description and Application Information

The MCIMX35 consists of the following major subsystems:

- ARM1136 Platform—AP domain
- SDMA Platform and EMI—Shared domain

2.1 Application Processor Domain Overview

The applications processor (AP) and its domain are responsible for running the operating system and applications software, providing the user interface, and supplying access to integrated and external peripherals. The AP domain is built around an ARM1136JF-S core with 16-Kbyte instruction and data L1 caches, an MMU, a 128-Kbyte L2 cache, a multiported crossbar switch, and advanced debug and trace interfaces.

The i.MX35 core is intended to operate at a maximum frequency of 532 MHz to support the required multimedia use cases. Furthermore, an image processing unit (IPU) is integrated into the AP domain to offload the ARM11 core from performing functions such as color space conversion, image rotation and scaling, graphics overlay, and pre- and post-processing.

The functionality of AP Domain peripherals includes the user interface; the connectivity, display, security, and memory interfaces; and 128 Kbytes of multipurpose SRAM.

2.2 Shared Domain Overview

The shared domain is composed of the shared peripherals, a smart DMA engine (SDMA) and a number of miscellaneous modules. For maximum flexibility, some peripherals are directly accessible by the SDMA engine.

The MCIMX35 has a hierarchical memory architecture including L1 caches and a unified L2 cache. This reduces the bandwidth demands for the external bus and external memory. The external memory subsystem supports a flexible external memory system, including support for SDRAM (SDR, DDR2 and mobile DDR) and NAND Flash.

2.3 Advanced Power Management Overview

To address the continuing need to reduce power consumption, the following techniques are incorporated in the MCIMX35:

- Clock gating
- Power gating
- Power-optimized synthesis
- Well biasing

The insertion of gating into the clock paths allows unused portions of the chip to be disabled. Because static CMOS logic consumes only leakage power, significant power savings can be realized.

"Well biasing" is applying a voltage that is greater than V_{dd} to the nwells, and one that is lower than V_{ss} to the pwells. The effect of applying this well back bias voltage reduces the subthreshold channel leakage. For the 90-nm digital process, it is estimated that the subthreshold leakage is reduced by a factor of ten over the nominal leakage. Additionally, the supply voltage for internal logic can be reduced from 1.4 V to 1.22 V.

2.4 ARM11 Microprocessor Core

The CPU of the i.MX35 is the ARM1136JF-S core, based on the ARM v6 architecture. This core supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes) and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features are as follows:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline

- Branch prediction with return stack
- Low-interrupt latency
- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a nonblocking data cache with hit-under-miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector floating point co-processor (VFP) for 3D graphics and hardware acceleration of other floating-point applications
- ETM™ and JTAG-based debug support

Table 2 summarizes information about the i.MX35 core.

Table 2. i.MX35 Core

Core Acronym	Core Name	Brief Description	Integrated Memory Features
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 x 5 multi-layer AHB crossbar switch (MAX), and a vector floating processor (VFP). The i.MX35 provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16-Kbyte instruction cache • 16-Kbyte data cache • 128-Kbyte L2 cache • 32-Kbyte ROM • 128-Kbyte RAM

2.5 Module Inventory

Table 3 shows an alphabetical listing of the modules in the MCIMX35. For extended descriptions of the modules, see the MCIMX35 reference manual.

Table 3. Digital and Analog Modules

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
1-WIRE	1-Wire interface	ARM	ARM1136 platform peripherals	1-Wire provides the communication line to a 1-Kbit add-only memory. the interface can send or receive 1 bit at a time.
ASRC	Asynchronous sample rate converter	SDMA	Connectivity peripherals	The ASRC is designed to convert the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. It supports a concurrent sample rate conversion of about –120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates.
ATA	ATA module	SDMA	Connectivity peripherals	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disk drives and ATAPI optical disk drives. It interfaces with the ATA device over a number of ATA signals.

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
AUDMUX	Digital audio mux	ARM	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CAN(2)	CAN module	ARM	Connectivity peripherals	The CAN protocol is primarily designed to be used as a vehicle serial data bus running at 1 Mbps.
CCM	Clock control module	ARM	Clocks	This block generates all clocks for the peripherals in the SDMA platform. The CCM also manages ARM1136 platform low-power modes (WAIT, STOP), disabling peripheral clocks appropriately for power conservation, and provides alternate clock sources for the ARM1136 and SDMA platforms.
CSPI(2)	Configurable serial peripheral interface	SDMA, ARM	Connectivity peripherals	This module is a serial interface equipped with data FIFOs; each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
ECT	Embedded cross trigger	SDMA, ARM	Debug	ECT (embedded cross trigger) is an IP for real-time debug purposes. It is a programmable matrix allowing several subsystems to interact with each other. ECT receives signals required for debugging purposes (from cores, peripherals, buses, external inputs, and so on) and propagates them (propagation programmed through software) to the different debug resources available within the SoC.
EMI	External memory interface	SDMA	External memory interface	The EMI module provides access to external memory for the ARM and other masters. It is composed of the following main submodules: M3IF—provides arbitration between multiple masters requesting access to the external memory. SDRAM CTRL—interfaces to mDDR, DDR2 (4-bank architecture type), and SDR interfaces. NANDFC—provides an interface to NAND Flash memories. WEIM—interfaces to NOR Flash and PSRAM.
EPIT(2)	Enhanced periodic interrupt timer	ARM	Timer peripherals	Each EPIT is a 32-bit “set-and-forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.
I^2C(3)	I^2C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: Up to eight output sources multiplexed per pin Up to four destinations for each input pin Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: Preprocessing of data from the sensor or from the external system memory Postprocessing of data from the external system memory Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms Displaying video and graphics on a synchronous (dumb or memory-less) display Displaying video and graphics on an asynchronous (smart) display Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypad port	ARM	Connectivity peripherals	Can be used for either keypad matrix scanning or general purpose I/O.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.
OSC24M	OSC24M—24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).
MPLL PPLL	Digital phase-locked loops	SDMA	Clocks	DPLLs are used to generate the clocks: MCU PLL (MPLL)—programmable Peripheral PLL (PPLL)—programmable
PWM	Pulse-width modulator	ARM	ARM1136 platform peripherals	The pulse-width modulator (PWM) is optimized to generate sound from stored sample audio images; it can also generate tones.
RTC	Real-time clock	ARM	Clocks	Provides the ARM1136 platform with a clock function (days, hours, minutes, seconds) and includes alarm, sampling timer, and minute stopwatch capabilities.

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
SDMA	Smart DMA engine	SDMA	System controls	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels and has an interface to connect to the ARM1136 platform subsystem, EMI interface, and the peripherals.
SJC	Secure JTAG controller	ARM	Pins	The secure JTAG controller (SJC) provides debug and test control with maximum security.
SPBA	SDMA peripheral bus arbiter	SDMA	System controls	The SPBA controls access to the SDMA peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
S/PDIF	Serial audio interface	SDMA	Connectivity peripherals	Sony/Philips digital transceiver interface
SSI(2)	Synchronous serial interface	SDMA, ARM(2)	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor connected to it to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the I^2C sound (I^2S) bus standard. The SSIs interface to the AUDMUX for flexible audio routing.
UART(3)	Universal asynchronous receiver/transmitters	ARM(UART1,2) SDMA(UART3)	Connectivity peripherals	Each UART provides serial communication capability with external devices through an RS-232 cable using the standard RS-232 non-return-to-zero (NRZ) encoding format. Each module transmits and receives characters containing either 7 or 8 bits (program-selectable). Each UART can also provide low-speed IrDA compatibility through the use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission).
USBOH	High-speed USB on-the-go	SDMA	Connectivity peripherals	The USB module provides high performance USB on-the-go (OTG) functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 low pin count specification. The module has DMA capabilities handling data transfer between internal buffers and system memory.
WDOG	Watchdog modules	ARM	Timer peripherals	Each module protects against system failures by providing a method of escaping from unexpected events or programming errors. Once activated, the timer must be serviced by software on a periodic basis. If servicing does not take place, the watchdog times out and then either asserts a system reset signal or an interrupt request signal, depending on the software configuration.

[1] ARM = ARM1136 platform, SDMA = SDMA platform

3 Signal Descriptions: Special Function Related Pins

Some special functional requirements are supported in the MCIMX35 device. The details about these special functions and the corresponding pad names are listed in Table 4.

Table 4. Special Function Related Pins

Function Name	Pad Name	Mux Mode	Detailed Description
External ARM Clock	EXT_ARMCLK	ALT0	External clock input for ARM clock.
External Peripheral Clock	I2C1_CLK	ALT6	External peripheral clock source.
External 32-kHz Clock	CAPTURE	ALT4	External clock input of 32 kHz, used when the internal 24M Oscillator is powered off, which could be configured either from CAPTURE or CSPI1_SS1.
	CSPI1_SS1	ALT2	
Clock Out	CLKO	ALT0	Clock-out pin from CCM, clock source is controllable and can also be used for debug.
Power Ready	GPIO1_0	ALT1	PMIC power-ready signal, which can be configured either from GPIO1_0 or TX1.
	TX1	ALT1	
Tamper Detect	GPIO1_1	ALT6	Tamper-detect logic is used to issue a security violation. This logic is activated if the tamper-detect input is asserted. Tamper-detect logic is enabled by the bit of IOMUXC_GPRA[2]. After enabling the logic, it is impossible to disable it until the next reset.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 5 for a quick reference to the individual tables and sections.

Table 5. i.MX35 Chip-Level Conditions

Characteristics	Table / Location
Absolute Maximum Ratings	Table 6 on page 12
MCIMX35 Operating Ranges	Table 7 on page 12
Interface Frequency	Table 8 on page 13

CAUTION

Stresses beyond those listed in Table 6, "Absolute Maximum Ratings," on page 12 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 7, "MCIMX35 Operating Ranges," on page 12 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage (Core)	VDD_{max}[1]	–0.5	1.47	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input Voltage Range	V_{Imax}	–0.5	3.6	V
Storage Temperature	$T_{storage}$	–40	125	°C
ESD Damage Immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard.

3 Corner pins max. 750 V.

4.1.1 MCIMX35 Operating Ranges

Table 7 provides the recommended operating ranges. The term NVCC in this section refers to the associated supply rail of an input or output.

Table 7. MCIMX35 Operating Ranges

Symbol	Parameter	Min.	Typical	Max.	Units
VDD	Core Operating Voltage 0 < f_{ARM} < 400 MHz	1.22	—	1.47	V
	Core Operating Voltage 0 < f_{ARM} < 532MHz	1.33	—	1.47	V
	State Retention Voltage	1	—	—	V
NVCC_EMI1,2,3	EMI[1]	1.7	—	3.6	V
NVCC_CRM	WTDG, Timer, CCM, GPIO, CSPI1	1.75	—	3.6	V
NVCC_NANDF	NANDF	1.75	—	3.6	V
NVCC_ATA	ATA, USB generic	1.75	—	3.6	V
NVCC_SDIO	eSDHC1	1.75	—	3.6	V
NVCC_CSI	CSI, SDIO2	1.75	—	3.6	V
NVCC_JTAG	JTAG	1.75	—	3.6	V

Table 7. MCIMX35 Operating Ranges (continued)

Symbol	Parameter	Min.	Typical	Max.	Units
NVCC_LCDC	LCDC, TTM, I2C1	1.75	—	3.6	V
NVCC_MISC	I2Sx2,ESAI, I2C2, UART2, UART1, FEC	1.75	—	3.6	V
NVCC_MLB[2]	MLB	1.75	—	3.6	V
PHY1_VDDA	USB OTG PHY	3.17	3.3	3.43	V
USBPHY1_VDDA_BIAS	USB OTG PHY	3.17	3.3	3.43	V
USBPHY1_UPLLVDD	USB OTG PHY	3.17	3.3	3.43	V
PHY2_VDD	USB HOST PHY	3.0	3.3	3.6	V
OSC24M_VDD	OSC24M	3.0	3.3	3.6	V
OSC_AUDIO_VDD	OSC_AUDIO	3.0	3.3	3.6	V
MVDD	MPLL	1.4	—	1.65	V
PVDD	PPLL	1.4	—	1.65	V
FUSE_VDD[3]	Fusebox program supply voltage	3.0	3.6	3.6	V
T_A	Operating Ambient Temperature Range	–20	—	70	°C

1 EMI I/O interface power supply should be set up according to external memory. For example, if using SDRAM then NVCC_EMI1,2,3 should all be set at 3.3 V (typ.). If using MDDR or DDR2, NVC_EMI1,2,3 must be set at 1.8 V (typ.).

2 MLB Interface I/O pads can be programmed to function as GPIO for the consumer and industrial parts by setting NVCC_MLB to 1.8 or 3.3V. NVCC_MLB can be left floating.

3 The Fusebox read supply is connected to supply of the full speed USBPHY. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming.

4.1.2 Interface Frequency Limits

Table 8 provides information on interface frequency limits.

Table 8. Interface Frequency

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz

4.2 Power Modes

Table 9 provides descriptions of the power modes of the MCIMX35 processor.

Table 9. MCIMX35 Power Modes

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Wait	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is active. L2 cache is kept powered. MCU PLL is on (400 MHz) PER PLL is off (can be configured) (default: 300 MHz) Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured). RNGC internal osc is off.	16 µA	44 µA	7.2 µA	13.2 µA	1.2 µA	2.2 µA
Doze	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted. L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is on(400 MHz) PER PLL is off (can be configured). (300Mhz). Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured) RNGC internal osc is off	TBD	TBD	TBD	TBD	TBD	TBD
Stop	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24MHz is on OSC audio is off RNGC internal osc is off	790 µA	TBD	40 µA	TBD	1 µA	TBD

Table 9. MCIMX35 Power Modes (continued)

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Static	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24MHz is on OSC audio is off RNGC internal osc is off	820 µA	15 µA	50 µA	800 µA	24 µA	35 µA
Note: Typical column: TA = 25°C **Note:** Maximum column TA = 70°C							

4.3 Supply Power-Up/Power-Down Requirements and Restrictions

This section provides power-up and power-down sequence guidelines for the i.MX35 processor.

CAUTION

Any i.MX35 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in irreversible damage to the i.MX35 processor (worst-case scenario).

NOTE

Deviation from these sequences can also result in one or both of the following:

- Excessive current during power-up phase
- Prevent the device from booting

4.3.1 Powering Up

The Power-up sequence should be completed as follows:

1. Assert Power on Reset ($\overline{\text{POR}}$).
2. Turn on digital logic domain and IO power supply: VDD*n*, NVCC*x*
3. Wait until VDD*n* and NVCC*x* power supplies are stable + 32 µs.
4. Turn on all other power supplies: PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVDD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, FUSEVDD. Note: FUSEVDD shall be tied to GND if not programming fuse.

5. Deassert the $\overline{\text{POR}}$ signal.
6. Wait until PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVDD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, (FUSEVDD, optional). Power supplies are stable + 100 us.

4.3.2 Powering Down

The power-up sequence in reverse order is recommended for powering down. However, all power supplies can be shut down at the same time.

4.4 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 10. These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.168 mm, Core via plating 0.016 mm.
- Full array map design, but nearly all balls under die are power or ground.
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: k = 0.9 W/m K

Table 10. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	53	ºC/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	30	ºC/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	44	ºC/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	27	ºC/W
Junction to boards[2]	—	$R_{\theta JB}$	19	ºC/W
Junction to case (top)[3]	—	$R_{\theta JCtop}$	10	ºC/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	ºC/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

4.5 I/O Pad DC Electrical Characteristics

I/O pads are of two types: GPIO and DDR. DDR pads can be configured in three different drive strength modes: mobile DDR, SDRAM, and DDR2. The SDRAM and mobile DDR modes can be further customized at three drive strength levels: normal, high and max.Table 11 shows currents for the different DDR pad drive strength modes.

Table 11. DDR Pad Drive Strength Mode Current Levels

Drive Mode	Normal	High	Max
Mobile DDR	3.6 mA	7.2 mA	10.8 mA
SDRAM	4 mA	8 mA	12 mA
DDR2	—	—	13.4 mA

Table 12 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pads. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 12. I/O Pad DC Electrical Characteristics

Pad	DC Electrical Characteristics	Symbol	Test Condition	Min.	Nom.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh=–1mA Ioh=spec'ed Drive	NVCC–0.15 0.8*NVCC	—	—	V
	Low-level output voltage	Vol	Ioh=–1mA Ioh=spec'ed Drive	—	—	0.15 0.2*NVCC	V
	High-level output current for slow mode	Ioh	Voh=0.8*NVCC Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA
	High-level output current for fast mode	Ioh	Voh=0.8*NVCC Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA
	Low-level output current for slow mode	Iol	Voh=0.2*NVCC Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode	Iol	Voh=0.2*NVCC Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8V, 3.3V NVCC (for digital cells in input mode)	VIH	—	0.7*NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8V, 3.3V NVCC (for digital cells in input mode	VIL	—	–0.3V	—	0.2*NVCC	V
	Input Hysteresis	VHYS	NVCC = 1.8 NVCC = 2.5 NVCC = 3.3	TBD	—	TBD	V
	Schmitt trigger VT+	VT+	—	0.5NVCC	—		V
	Schmitt trigger VT-	VT-	—	—	—	0.5NVCC	V
	Pull-up resistor (22 KΩ PU)	Rpu	Vi = 0	—	22	—	KΩ
	Pull-up resistor (47 KΩ PU)	Rpu	Vi = 0	—	47	—	KΩ
	Pull-up resistor (100 KΩ PU)	Rpu	Vi = 0	—	100	—	KΩ
	Pull-down resistor (100 KΩ PD)	Rpd	Vi = NVCC	—	100	—	KΩ

Table 12. I/O Pad DC Electrical Characteristics (continued)

Pad	DC Electrical Characteristics	Symbol	Test Condition	Min.	Nom.	Max.	Unit
DDR2	High-level output voltage	Voh	—	NVCC–0.28	—	—	V
	Low-level output voltage	Vol	—		—	0.28	V
	Output min. source current	Ioh	—	–13.4	—	—	mA
	Output min. sink current	Iol	—	13.4	—	—	mA
	DC input logic high	VIH(dc)	—	NVCC/2+0.125	—	NVCC+0.3	V
	DC input logic low	VIL(dc)	—	–0.3 V	—	NVCC/2–0.125	V
	DC input signal voltage (for differential signal)	Vin(dc)	—	–0.3	—	NVCC+0.3	V
	DC differential input voltage	Vid(dc)	—	0.25	—	NVCC+0.6	V
	Termination voltage	Vtt	—	NVCC/2–0.04	NVCC/2	NVCC/2+0.04	V
	Input current (no pull-up/down)	IIN	—	—	TBD	TBD	nA
	Tri-state I/O supply current	Icc–NVCC	—	—	—	TBD	nA
	Tri-state core supply current	Icc–vddi	—	—	—	TBD	nA
Mobile DDR	High-level output voltage	—	I_{OH} = –1mA I_{OH} = spec'ed Drive	NVCC – 0.08 0.8*NVCC	—	—	V
	Low-level output voltage	—	I_{OL} = 1mA I_{OL} = spec'ed Drive	—	—	0.08 0.2*NVCC	V
	High-level output current	—	Voh=0.8*NVCCV Standard Drive High Drive Max. Drive	–3.6 –7.2 –10.8	—	—	mA
	Low-level output current	—	Vol=0.2*NVCCV Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA
	High-Level DC CMOS input voltage	VIH	—	0.7*NVCC	—	NVCC+0.3	V
	Low-Level DC CMOS input voltage	VIL	—	–0.3	—	0.2*NVCC	V
	Differential receiver VTH+	VTH+	—		—	100	mV
	Differential receiver VTH–	VTH–	—	–100	—		mV
	Input current (no pull-up/ down)	IIN	VI = 0 VI=NVCC	—	—	TBD	nA
	Tri-state I/O supply current	Icc–NVCC	VI = NVCC or 0	—	—	TBD	nA
	Tri-state core supply current	Icc–vddi	VI = VDD or 0	—	—	TBD	nA

Table 12. I/O Pad DC Electrical Characteristics (continued)

Pad	DC Electrical Characteristics	Symbol	Test Condition	Min.	Nom.	Max.	Unit
SDRAM	High-level output voltage	Voh	Ioh=spec'ed drive (Ioh=–4, –8, –12, –16 mA)	2.4	—	—	V
	Low-level output voltage	Vol	Ioh=spec'ed drive (Ioh=4, 8, 12, 16mA)	—	—	0.4	V
	High-level output current	Ioh	Standard drive High drive Max. drive	–4.0 –8.0 –12.0	—	—	mA
	Low-level output current e	Iol	Standard drive High drive Max. drive	4.0 8.0 12.0	—	—	mA
	High-level DC Input Voltage	VIH	—	2.0	—	3.6	V
	Low-level DC Input Voltage	VIL	—	–0.3V	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI=NVCC	—	—	TBD	nA
	Tri-state I/O supply current	Icc_ovtwdd	VI = NVCC or 0	—	—	TBD	nA
	Tri-state core supply current	Icc-vddi	VI = VDD or 0	—	—	TBD	nA

4.6 I/O Pad AC Electrical Characteristics

Figure 2 shows the load circuit for output pads. and Figure 3 shows the output pad transition time waveform.

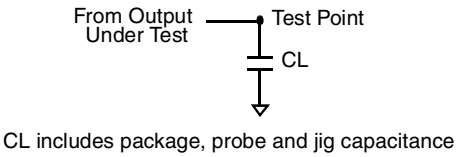


Figure 2. Load Circuit for Output Pad

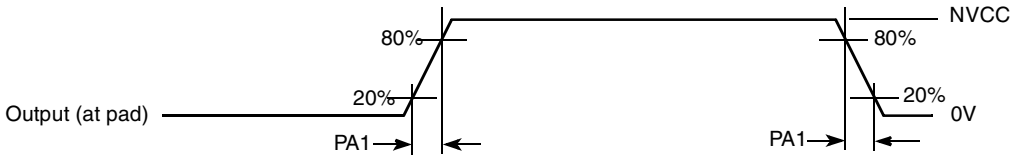


Figure 3. Output Pad Transition Time Waveform

4.6.1 AC Electrical Test Parameter Definitions

- AC electrical characteristics in Table 13 through Table 18 are not applicable for the output open drain pull-down driver.
- The dI/dt parameters are measured with the following methodology:
  - The zero voltage source is connected between pad and load capacitance.
  - The current (through this source) derivative is calculated during output transitions.

Table 13. AC Electrical Characteristics of GPIO Pads in Slow Slew Rate Mode [NVCC=3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall
Duty cycle	Fduty	—	40	—	60
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.79/1.12 0.49/0.73	1.30/1.77 0.84/1.23	2.02/2.58 1.19/1.58
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.48/0.72 0.27/0.42	0.76/1.10 0.41/0.62	1.17/1.56 0.63/0.86
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.25/0.40 0.14/0.21	0.40/0.59 0.21/0.32	0.60/0.83 0.32/0.44
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	15 16	36 38	76 80
Output pad di/dt (high drive)	tdit	25 pF 50 pF	8 9	20 21	45 47
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	4 4	10 10	22 23

Table 14. AC Electrical Characteristics of GPIO Pads in Slow Slew Rate Mode [NVCC=1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.30/0.42 0.20/0.29	0.54/0.73 0.35/0.50	0.91/1.20 0.60/0.80	V/ns
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.19/0.28 0.12/0.18	0.34/0.49 0.34/0.49	0.58/0/79 0.36/0.49	V/ns
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.12/0.18 0.07/0.11	0.20/0.30 0.11/0.17	0.34/0.47 0.20/0.27	V/ns
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	7 7	21 22	56 58	mA/ns
Output pad di/dt (high drive)	tdit	25 pF 50 pF	5 5	14 15	38 40	mA/ns
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	2 2	7 7	18 19	mA/ns

Table 15. AC Electrical Characteristics of GPIO Pads in Fast Slew Rate Mode for [NVCC=3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. rise/fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output pad di/dt (high drive)	tdit	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	22 23	52 55	116 121	mA/ns

Table 16. AC Electrical Characteristics, GPIO Pads in Fast Slew Rate Mode [NVCC=1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pad di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

Table 17. AC Electrical Characteristics of GPIO Pads in Slow Slew Rate Mode [NVCC=2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pad slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns

Table 17. AC Electrical Characteristics of GPIO Pads in Slow Slew Rate Mode [NVCC=2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pad slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pad di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

Table 18. AC Electrical Characteristics of GPIO Pads in Fast Slew Rate Mode [NVCC=2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pad slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pad slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pad slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pad di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.6.2 AC Electrical Characteristics for DDR Pads (DDR2, Mobile DDR, and SDRAM Modes)

Table 19. AC Electrical Characteristics of DDR Type IO Pads in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	133	—	MHz
Output pad slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pad di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 20. AC Requirements of DDR2 Pads

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC/2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC/2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC/2 – 0.125	NVCC/2 + 0.125	V

1 The Jedec SSTL_18 specification (JESD8–15a) for a SSTL interface for class II operation supersedes any specification in this document.

2 The typical value of Vox(ac) is expected to be about 0.5*NVCC and Vox(ac) is expected to track variation in NVCC. Vox(ac) indicates the voltage at which the differential output signal must cross. Cload=25 pF.

Table 21. AC Electrical Characteristics of DDR Type IO Pads in mDDR Mode, Fast Slew Rate

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	133	—	MHz
Output pad slew rate (max. drive)	tps	25pF 50pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pad slew rate (high drive)	tps	25pF 50pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pad slew rate (standard drive)	tps	25pF 50pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pad di/dt (max. drive)	tdit	25pF 50pF	64 69	171 183	407 432	mA/ns
Output pad di/dt (high drive)	tdit	25pF 50pF	37 39	100 106	232 246	mA/ns
Output pad di/dt (standard drive)	tdit	25pF 50pF	18 20	50 52	116 123	mA/ns

Table 22. AC Electrical Characteristics of DDR Type IO Pads in mDDR Mode, Slow Slew Rate

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	133	—	MHz
Output pad slew rate (max. drive)	tps	25pF 50pF	0.37/0.45 0.30/0.36	0.64/0.79 0.52/0.61	1.14/1.36 0.90/1.02	V/ns
Output pad slew rate (high drive)	tps	25pF 50pF	0.30/0.37 0.21/0.25	0.51/0.63 0.36/0.42	091/1.06 0.63/0.67	V/ns
Output pad slew rate (standard drive)	tps	25pF 50pF	0.22/0.26 0.13/0.16	0.37/0.44 0.23/0.26	0.65/0.72 0.39/0.40	V/ns
Output pad di/dt (max. drive)	tdit	25pF 50pF	65 70	171 183	426 450	mA/ns
Output pad di/dt (high drive)	tdit	25pF 50pF	31 33	82 87	233 245	mA/ns
Output pad di/dt (standard drive)	tdit	25pF 50pF	16 17	43 46	115 120	mA/ns

Table 23. AC Electrical Characteristics of DDR Type IO Pads in SDRAM Mode, Fast Slew Rate

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	125	—	MHz
Output pad slew rate (max. drive)	tps	25pF 50pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pad slew rate (high drive)	tps	25pF 50pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pad slew rate (standard drive)	tps	25pF 50pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pad di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

Table 24. AC Electrical Characteristics of DDR Type IO Pads in Mobile DDR Mode, Slow Slew Rate

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	125	—	MHz

Table 24. AC Electrical Characteristics of DDR Type IO Pads in Mobile DDR Mode, Slow Slew Rate

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad slew rate (max. drive)	tps	25pF 50pF	1.11/1.20 0.60/0.65	1.74/1.75 0.93/0.95	2.63/2.48 1.39/1.29	V/ns
Output pad slew rate (high drive)	tps	25pF 50pF	0.75/0.81 0.40/0.43	1.16/1.18 0.62/0.64	1.76/1.65 094/0.87	V/ns
Output pad slew rate (standard drive)	tps	25pF 50pF	0.38/0.41 0.20/0.22	0.59/0.61 0.31/0.32	0.89/0.83 0.47/0.43	V/ns
Output pad di/dt (max. drive)	tdit	25 pF 50 pF	89 95	202 213	435 456	mA/ns
Output pad di/dt (high drive)	tdit	25 pF 50 pF	60 63	135 142	288 302	mA/ns
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	29 31	67 70	144 150	mA/ns

4.7 Module-Level AC Electrical Specifications

This section contains the AC electrical information (including timing specifications) for different modules of the MCIMX35. The modules are listed in alphabetical order.

4.7.1 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. See the electrical specification for SSI.

4.7.2 CSPI AC Electrical Specifications

The MCIMX35 provides two CSPI modules. CSPI ports are multiplexed in the MCIMX35 with other pads. See the “External Signals and Multiplexing” chapter of the reference manual for more details.

Figure 4 and Figure 5 depict the master mode and slave mode timings of the CSPI, and Table 25 lists the timing parameters.

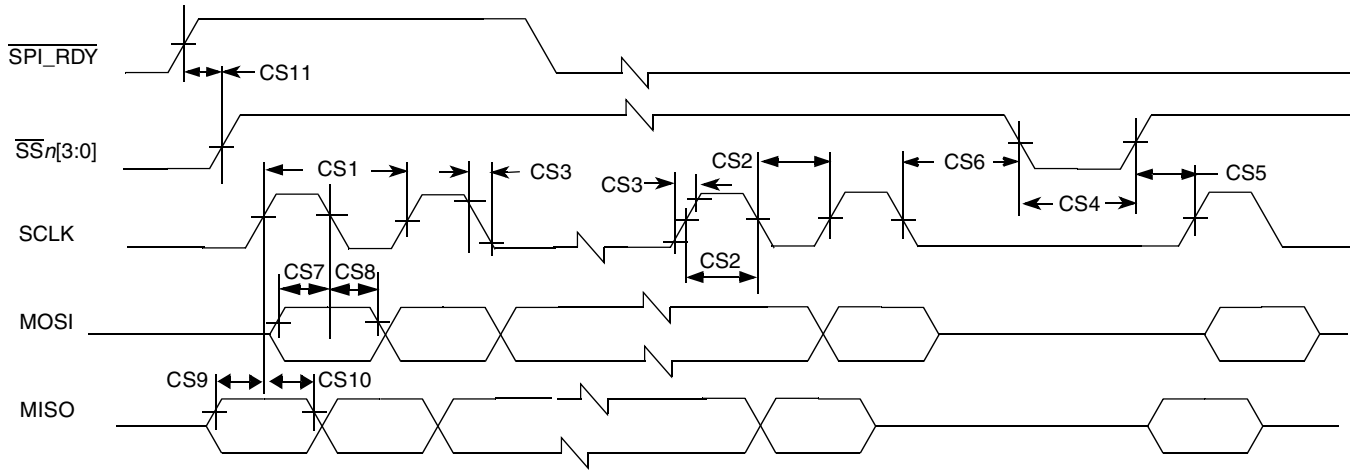


Figure 4. CSPI Master Mode Timing Diagram

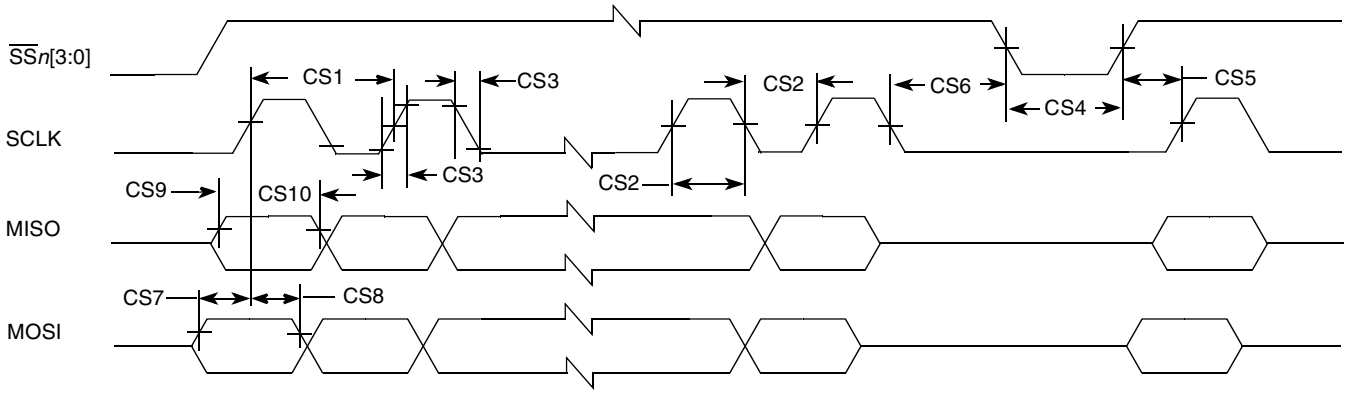


Figure 5. CSPI Slave Mode Timing Diagram

Table 25. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
CS1	SCLK cycle time	t_{clk}	60	—	ns
CS2	SCLK high or low time	t_{SW}	30	—	ns
CS3	SCLK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SS}n$[3:0] pulse width	t_{CSLH}	30	—	ns
CS5	$\overline{SS}n$[3:0] lead time (CS setup time)	t_{SCS}	30	—	ns
CS6	$\overline{SS}n$[3:0] lag time (CS hold time)	t_{HCS}	30	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns
CS10	MISO hold time	t_{Hmiso}	5	—	ns
CS11	$\overline{SPI\_RDY}$ setup time	t_{SDRY}	5	—	ns

4.7.3 DPLL Electrical Specifications

There are three PLLs inside the MCIMX35, all based on the same PLL design. The reference clock for these PLLs is normally generated from an external 24-MHz crystal connected to an internal oscillator via EXTAL24M and XTAL24 pads. It is also possible to connect an external 24-MHz clock directly to EXTAL24M, bypassing the internal oscillator.

DPLL specifications are listed in Table 26.

Table 26. DPLL Specifications

Parameter	Min.	Typ.	Max.	Unit	Comments
Reference clock frequency	10	24	100	MHz	
Max. allowed reference clock phase noise	—	—	0.03 0.01 0.15	2 Tdck[1]	Fmodulation <50 kHz 50 kHz<Fmodulation 300 Hz Fmodulation > 300 KHz
Frequency lock time (FOL mode or non-integer MF)	—	—	80	µs	—
Phase lock time	—	—	100	µs	—
Max. allowed PL voltage ripple	—	—	150 100 150	mV	Fmodulation < 50 kHz 50 kHz < Fmodulation 300 Hz Fmodulation > 300 KHz

[1] There are two PLL are used in the MCIMX35, MPLL and PPLL. Both are based on same DPLL design.

4.7.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

Figure 6 depicts the TRACECLK timings of ETM, and Table 27 lists the timing parameters.

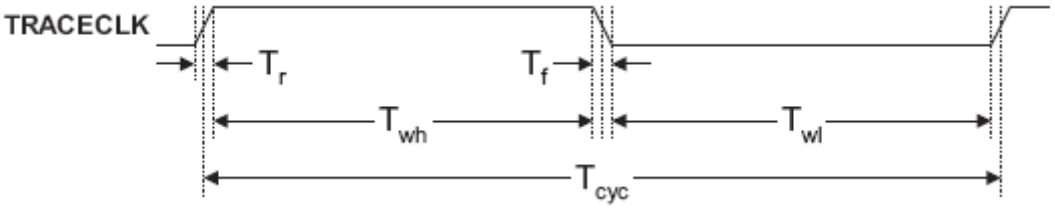


Figure 6. ETM TRACECLK Timing Diagram

Table 27. ETM TRACECLK Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns

Table 27. ETM TRACECLK Timing Parameters (continued)

ID	Parameter	Min.	Max.	Unit
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 7 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 28 lists the timing parameters.

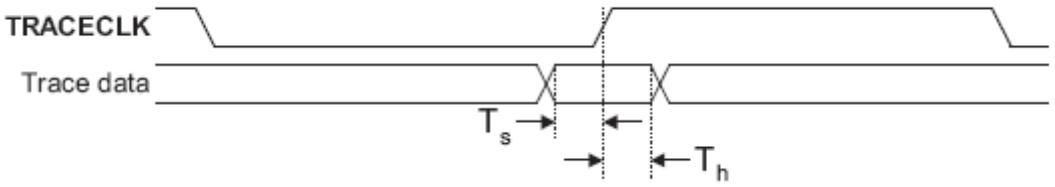


Figure 7. Trace Data Timing Diagram

Table 28. ETM Trace Data Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.7.4.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 7. The same T_s and T_h parameters from Table 28 still apply with respect to the falling edge of the TRACECLK signal.

4.7.5 EMI Electrical Specifications

This section provides electrical parametrics and timing for the EMI module.

4.7.5.1 NAND Flash Controller Interface (NFC)

The MCIMX35 NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 8, Figure 9, Figure 10, and Figure 11 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 29 lists the timing parameters.

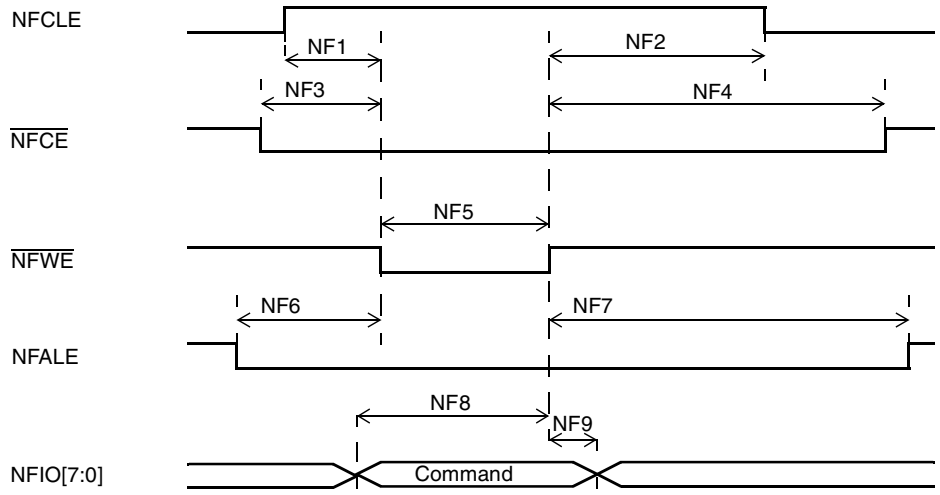


Figure 8. Command Latch Cycle Timing Diagram

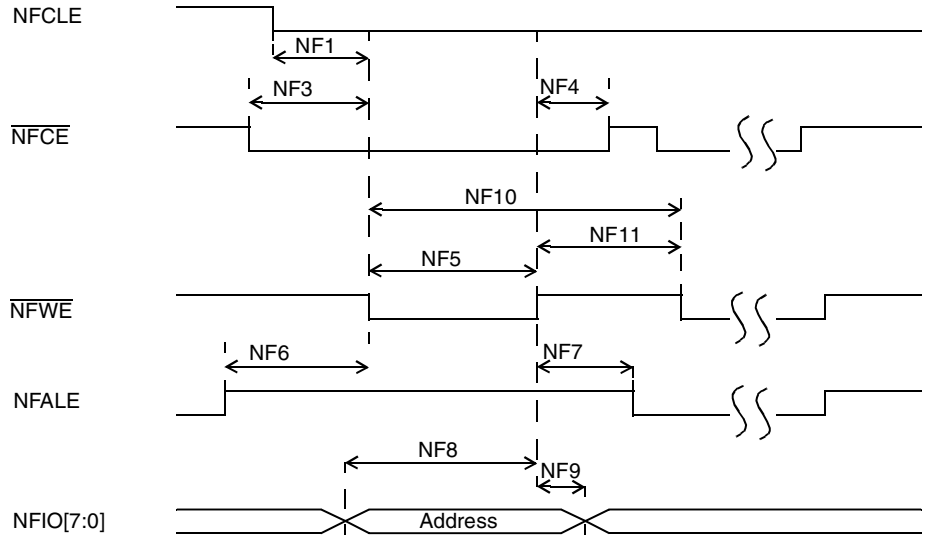


Figure 9. Address Latch Cycle Timing Diagram

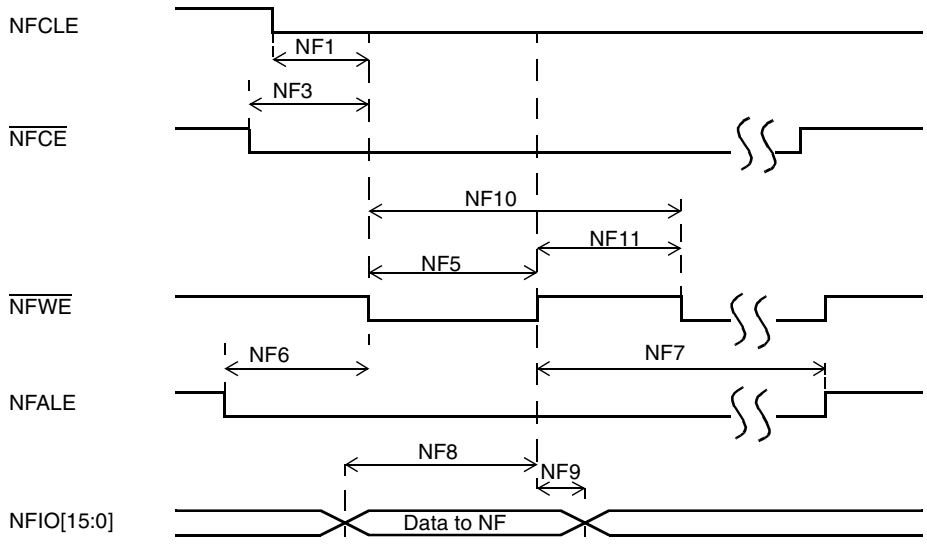


Figure 10. Write Data Latch Cycle Timing Diagram

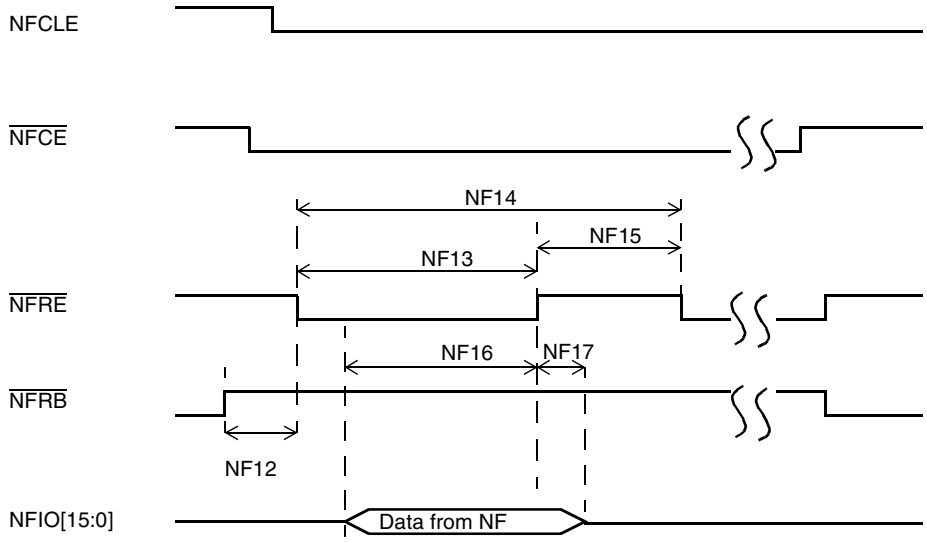


Figure 11. Read Data Latch Cycle Timing Diagram

Table 29. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T–1.0 ns	—	29	—	ns
NF2	NFCLE hold time	tCLH	T–2.0 ns	—	28	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	T–1.0 ns	—	29	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	T–2.0 ns	—	28	—	ns

Table 29. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{\text{NF\_WP}}$ pulse width	tWP	T–1.5 ns		28.5		ns
NF6	NFALE setup time	tALS	T	—	30	—	ns
NF7	NFALE hold time	tALH	T–3.0 ns	—	27	—	ns
NF8	Data setup time	tDS	T	—	30	—	ns
NF9	Data hold time	tDH	T–5.0 ns	—	25	—	ns
NF10	Write cycle time	tWC	2T		60		ns
NF11	$\overline{\text{NFWE}}$ hold time	tWH	T–2.5 ns		27.5		ns
NF12	Ready to $\overline{\text{NFRE}}$ low	tRR	6T	—	180	—	ns
NF13	$\overline{\text{NFRE}}$ pulse width	tRP	1.5T	—	45	—	ns
NF14	READ cycle time	tRC	2T	—	60	—	ns
NF15	$\overline{\text{NFRE}}$ high hold time	tREH	0.5T–2.5 ns		12.5	—	ns

Table 29. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF16	Data setup on READ	tDSR	N/A		10	—	ns
NF17	Data hold on READ	tDHR	N/A		0	—	ns

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification listed in Table 26, "DPLL Specifications," on page 28.

NOTE

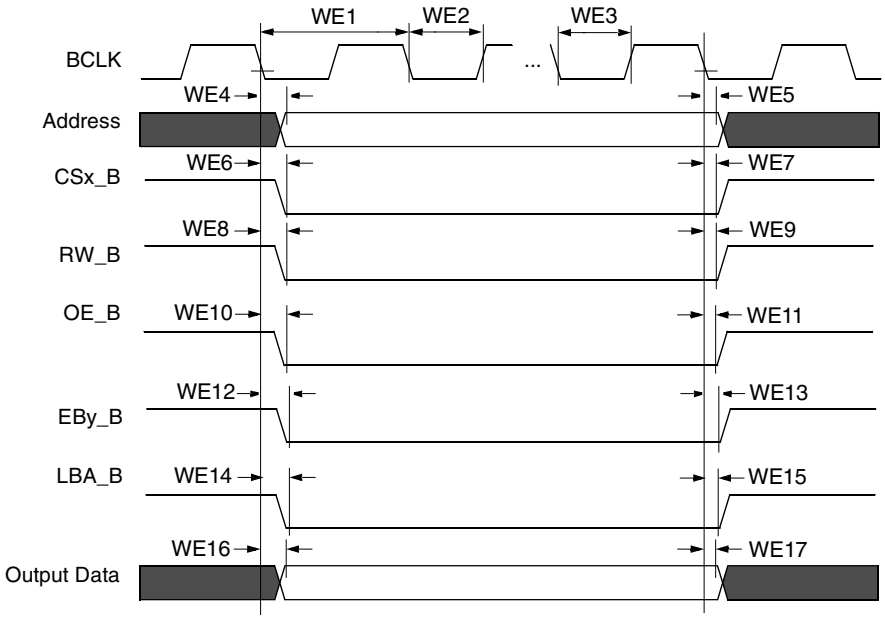
High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.7.5.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clocks related to the BCLK rising edge or falling edge according to the corresponding assertion or negation control fields. The address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 12 depicts the timing of the WEIM module, and Table 30 lists the timing parameters.

WEIM Output Timing



WEIM Input Timing

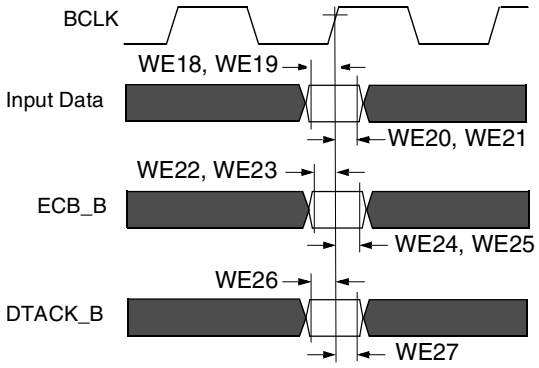


Figure 12. WEIM Bus Timing Diagram

Table 30. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	7.5	—	ns
WE2	BCLK low-level width[2]	3.0	—	ns
WE3	BCLK high-level width[2]	3.0	—	ns
WE4	Clock fall to address valid	0.7	2.0	ns
WE5	Clock rise/fall to address invalid	0.7	2.5	ns
WE6	Clock rise/fall to CSx_B] valid	0.4	2.3	ns
WE7	Clock rise/fall to CSx_B] invalid	0.4	2.3	ns

Table 30. WEIM Bus Timing Parameters[1] (continued)

ID	Parameter	Min.	Max.	Unit
WE8	Clock rise/fall to RW_B Valid	0.9	2.6	ns
WE9	Clock rise/fall to RW_B Invalid	0.9	2.6	ns
WE10	Clock rise/fall to OE_B Valid	1.2	2.5	ns
WE11	Clock rise/fall to OE_B Invalid	1.2	2.5	ns
WE12	Clock rise/fall to EBy_B Valid	0.7	2.4	ns
WE13	Clock rise/fall to EBy_B Invalid	0.7	2.4	ns
WE14	Clock rise/fall to LBA_B Valid	1.0	2.8	ns
WE15	Clock rise/fall to LBA_B Invalid	1.0	2.8	ns
WE16	Clock rise/fall to Output Data Valid	1.0	3.0	ns
WE17	Clock rise to Output Data Invalid	1.0	3.0	ns
WE18	Input Data Valid to Clock rise, FCE=1	1.2	—	ns
WE19	Input Data Valid to Clock rise, FCE=0	6.9	—	ns
WE20	Clock rise to Input Data Invalid, FCE=1	0.2	—	ns
WE21	Clock/k rise to Input Data Invalid, FCE=0	2.4	—	ns
WE22	ECB_B setup time, FCE=1	1.1	—	ns
WE23	ECB_B setup time, FCE=0	7.2	—	ns
WE24	ECB_B hold time, FCE=1	0	—	ns
WE25	ECB_B hold time, FCE=0	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	–3.2	—	ns

1 “High” is defined as 80% of signal value, and “low” is defined as 20% of signal value.

2 BCLK parameters are measured from the 50% point. For example, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

NOTE

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is set to maximum drive.

Recommended drive strength for all controls, address and BCLK is set to maximum drive.

Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, and Figure 18 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 30 for specific control parameter settings.

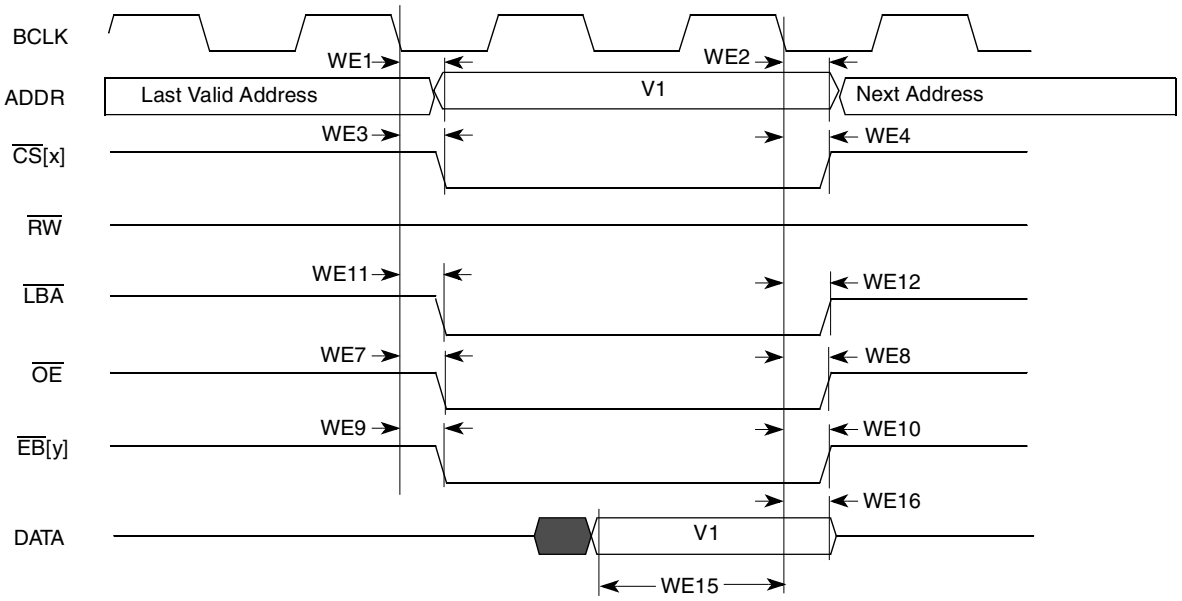


Figure 13. Asynchronous Memory Timing Diagram for Read Access—WSC=1

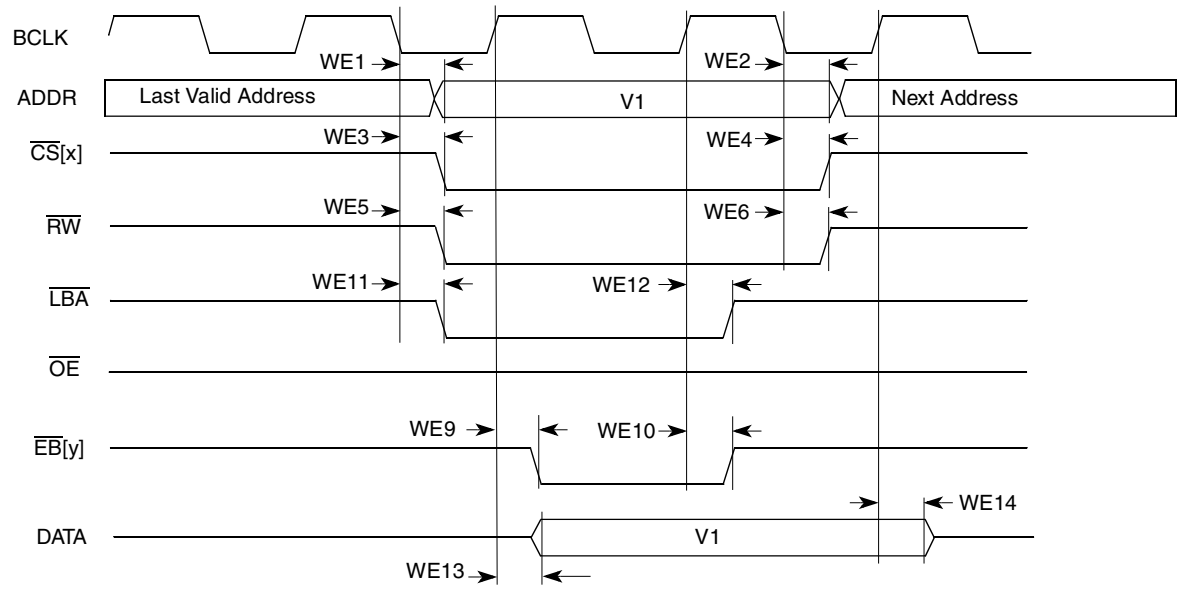


Figure 14. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

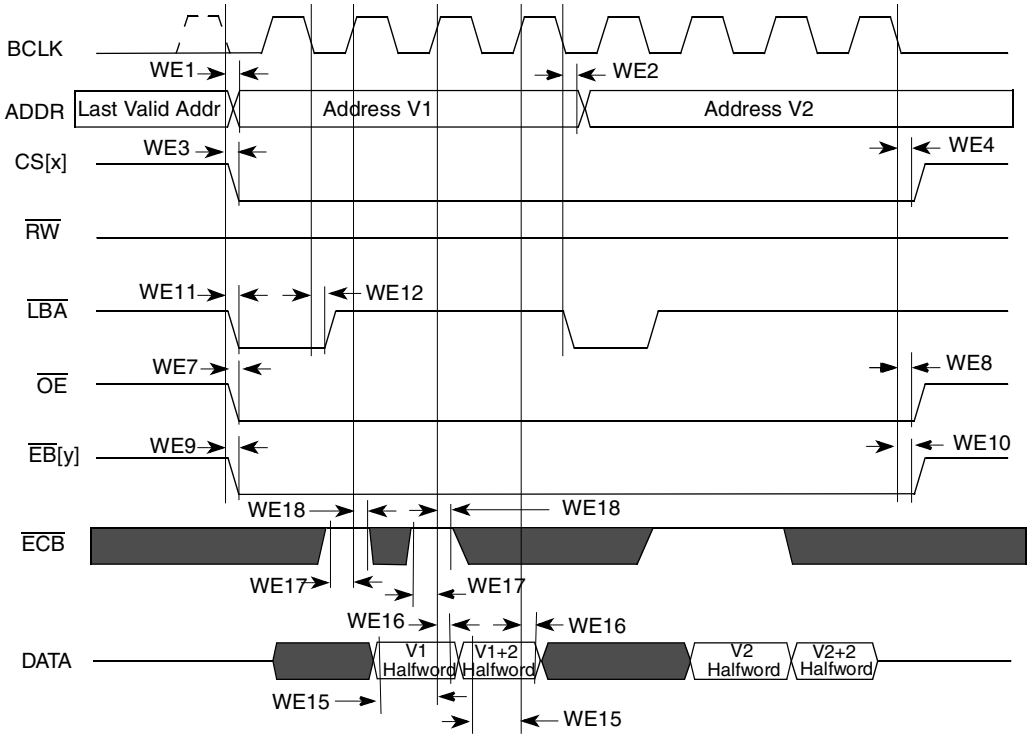


Figure 15. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses—WSC=2, SYNC=1, DOL=0

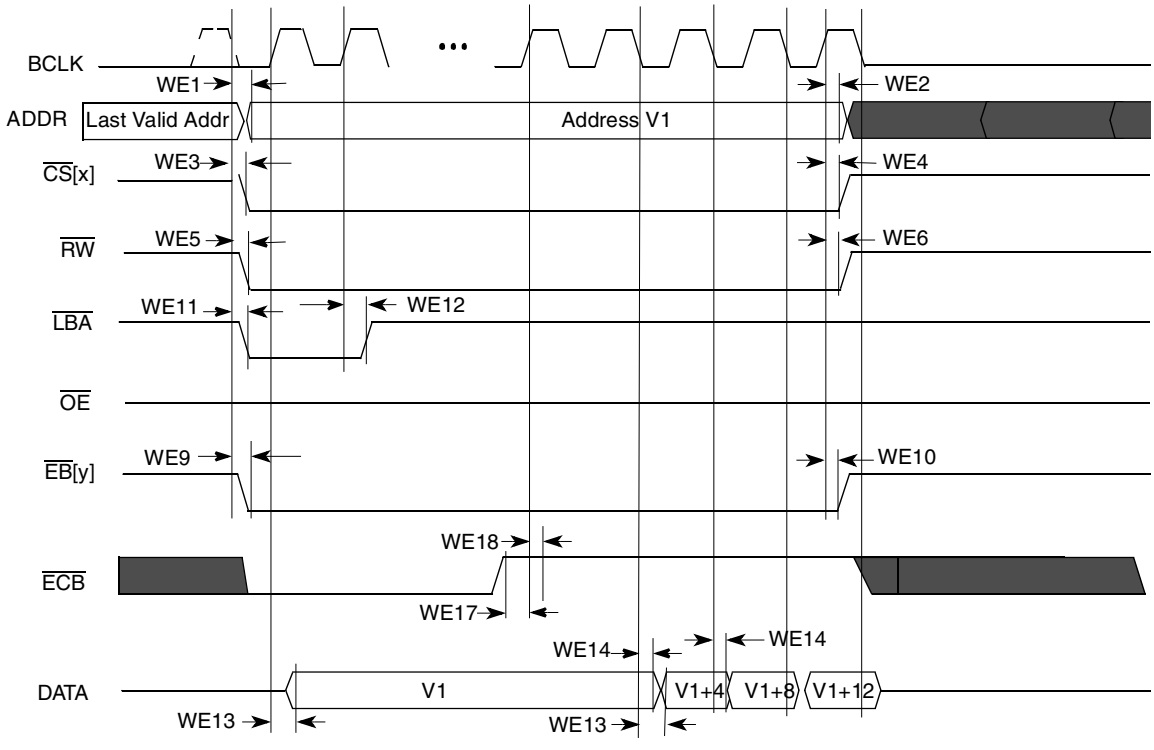


Figure 16. Synchronous Memory TIming Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1

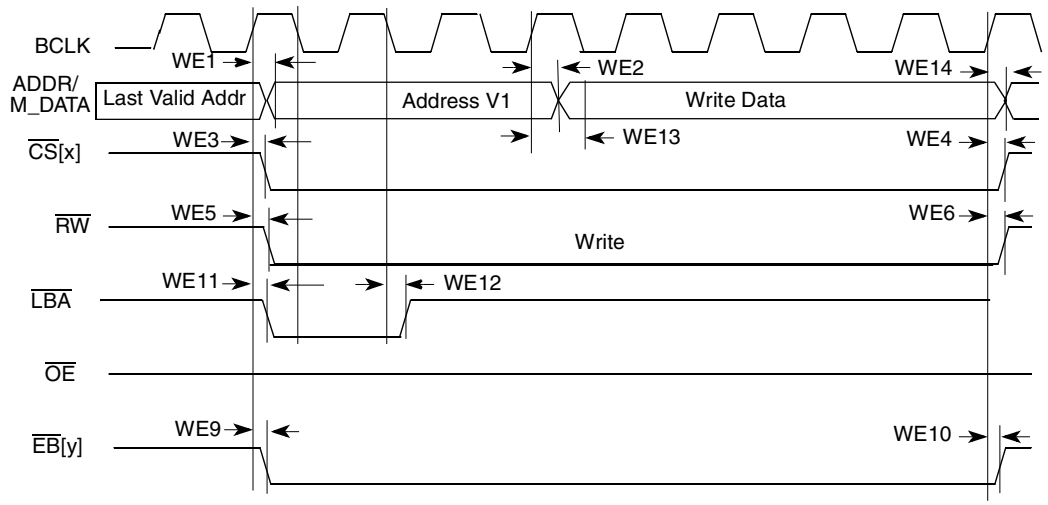


Figure 17. Muxed A/D Mode Timing Diagram for Asynchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

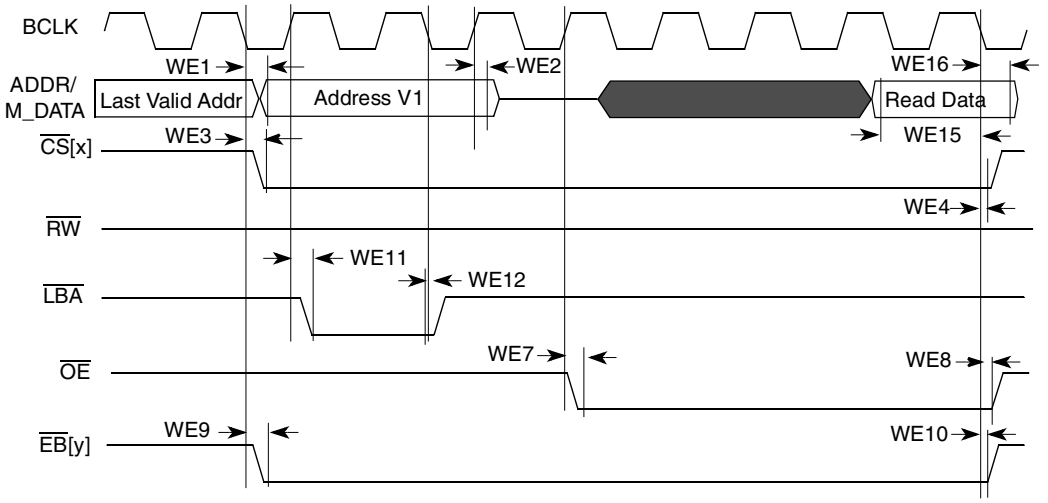


Figure 18. Muxed A/D Mode Timing Diagram for Asynchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

4.7.5.3 ESDCTL Electrical Specifications

Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, and Figure 24 depict the timings pertaining to the ESDCTL module, which interfaces with mobile DDR or SDR SDRAM. Table 31, Table 32, Table 33, Table 34, Table 35, and Table 36 list the timing parameters.

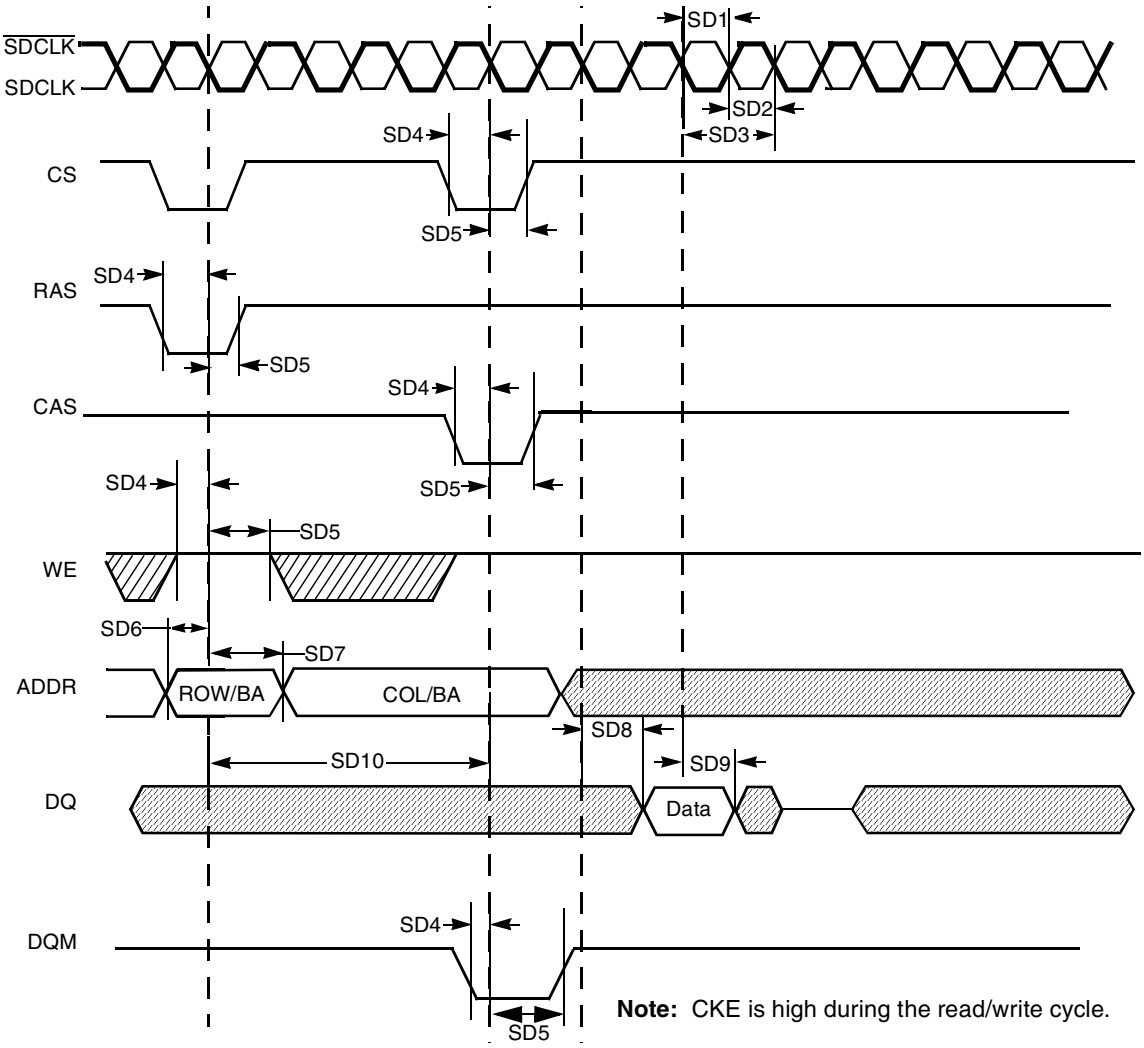


Figure 19. SDRAM Read Cycle Timing Diagram

Table 31. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

Table 31. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD9	Data out hold time[1]	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 35 and Table 36.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 31 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

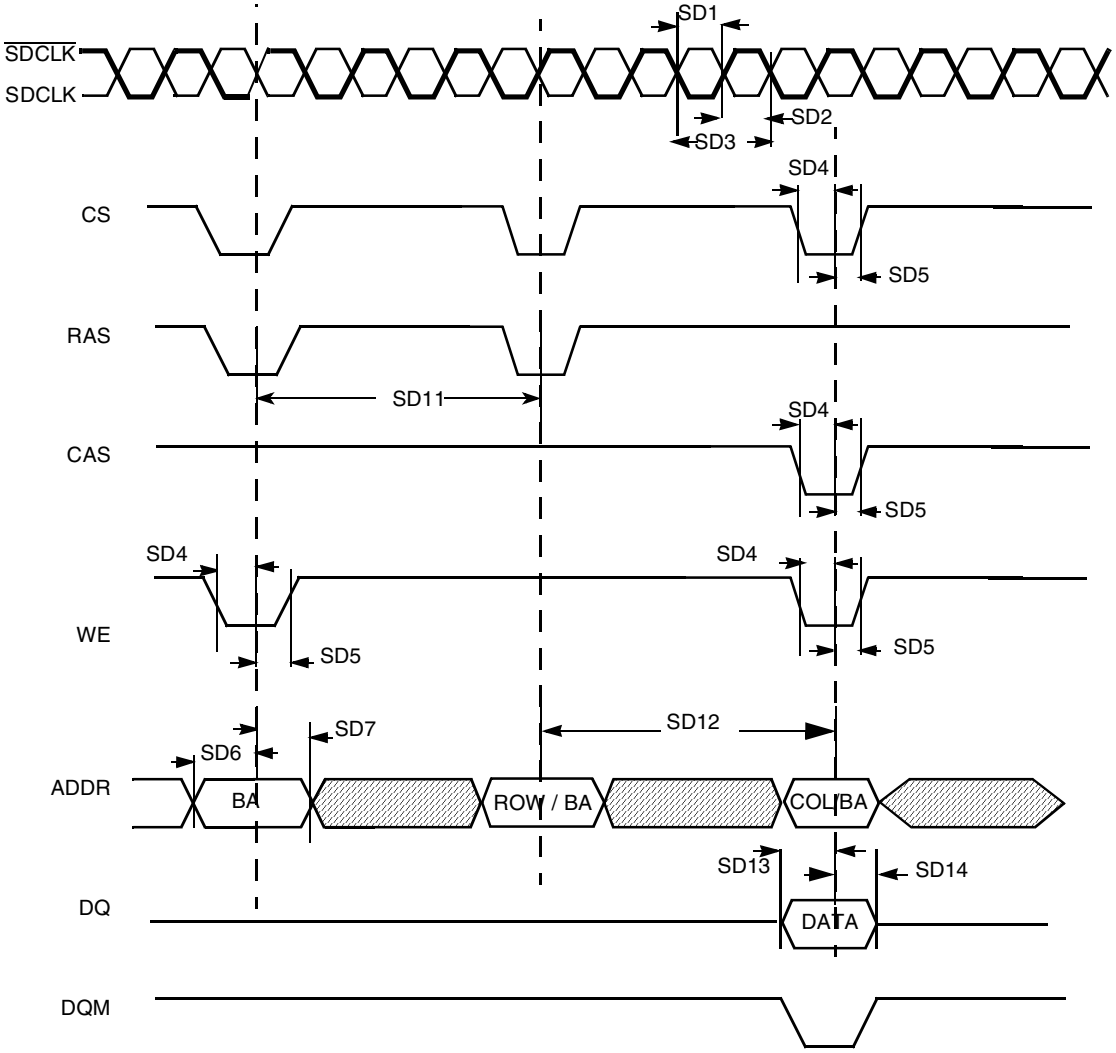


Figure 20. SDR SDRAM Write Cycle Timing Diagram

Table 32. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD11	Precharge cycle period[1]	tRP	1	4	clock
SD12	Active to read/write command delay[1]	tRCD	1	8	clock

Table 32. SDR SDRAM Write Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

[1] SD11 and SD12 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 32 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

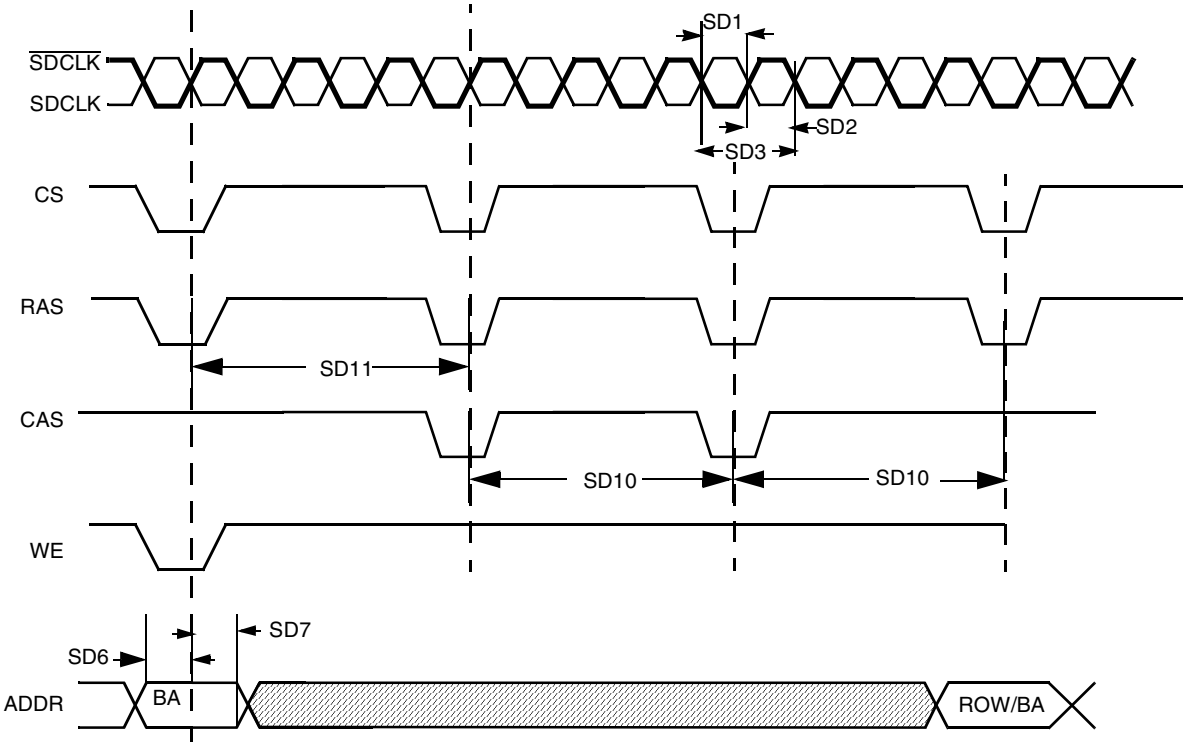


Figure 21. SDRAM Refresh Timing Diagram

Table 33. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM}}$ clock low-level width	tCL	3.4	4.1	ns

Table 33. SDRAM Refresh Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 33 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

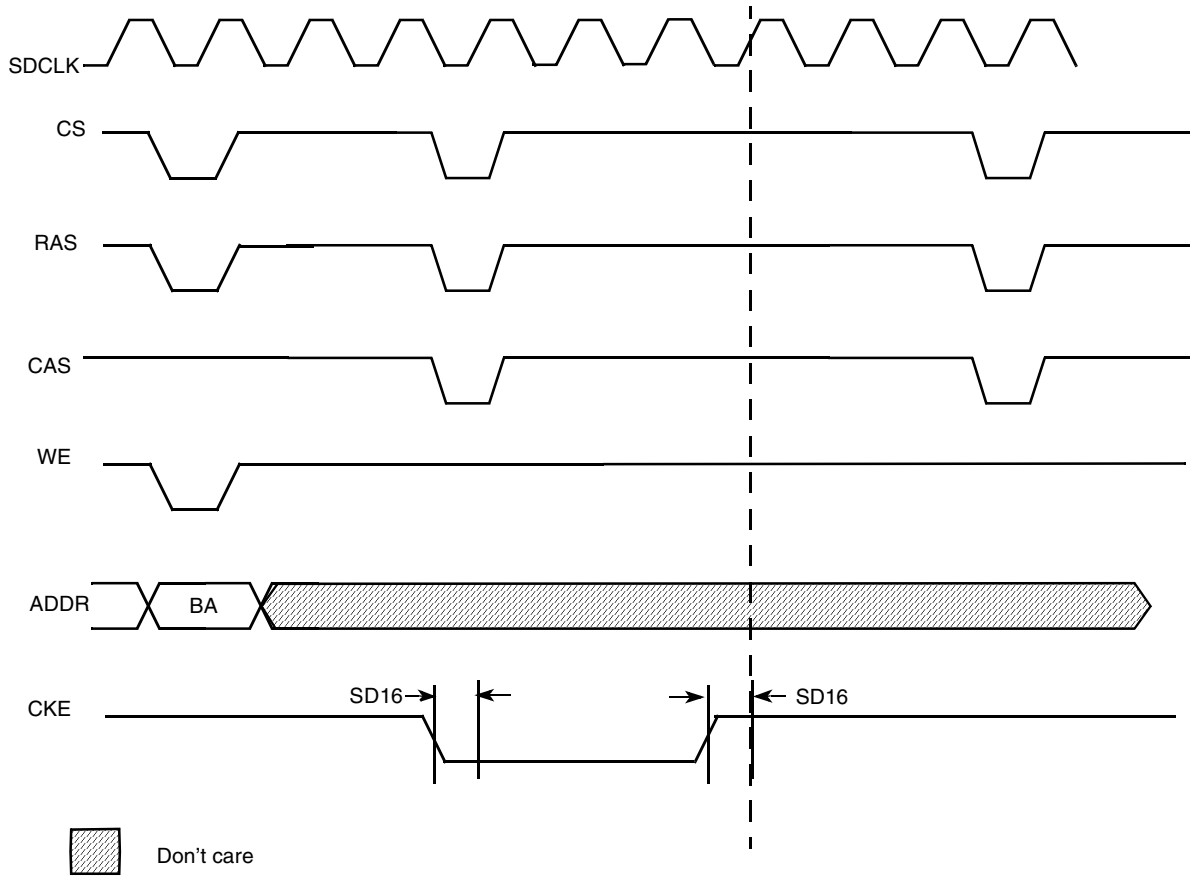


Figure 22. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 34. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

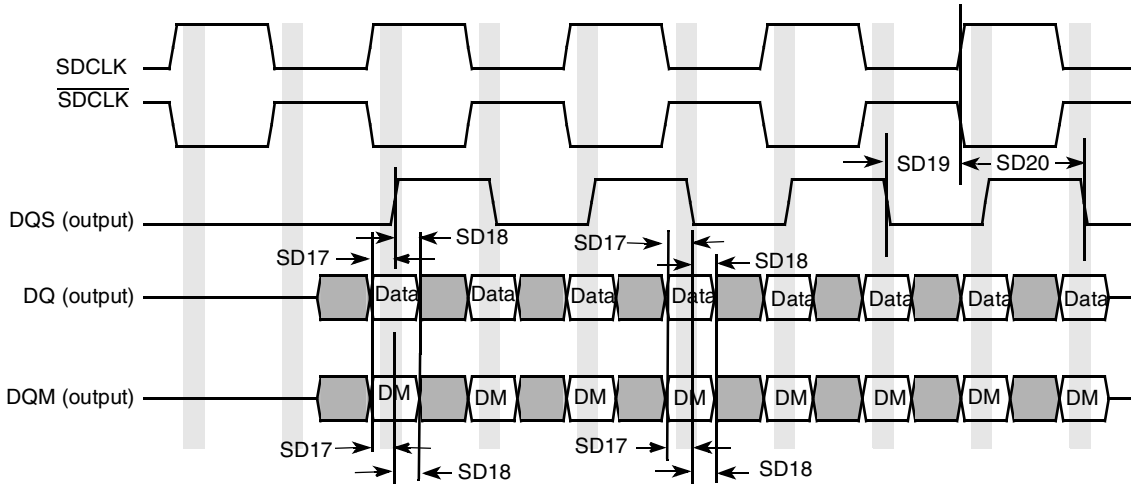


Figure 23. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 35. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

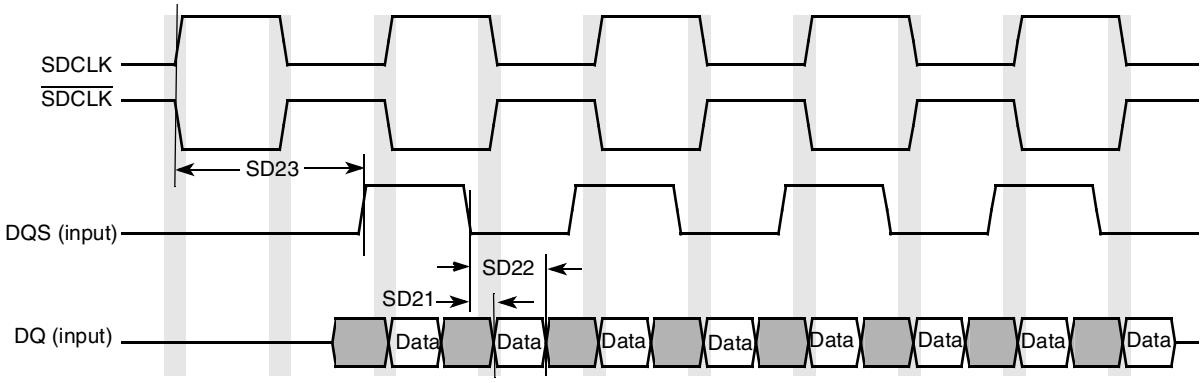


Figure 24. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 36. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

4.7.6 Enhanced Serial Audio Interface (ESAI) Timing Specifications

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 37 shows the interface timing values. The number field in the table refers to timing signals found in Figure 25 and Figure 26.

Table 37. Enhanced Serial Audio Interface Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	—	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 —	ns
64	Clock low period • For internal clock • For external clock	—	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 —	ns
65	SCKR rising edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns

Table 37. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
80	SCKT rising edge to FST out (wr) high[5]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	—	—	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	—	—	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	—	—	4.0 5.0	— —	x ck i ck	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

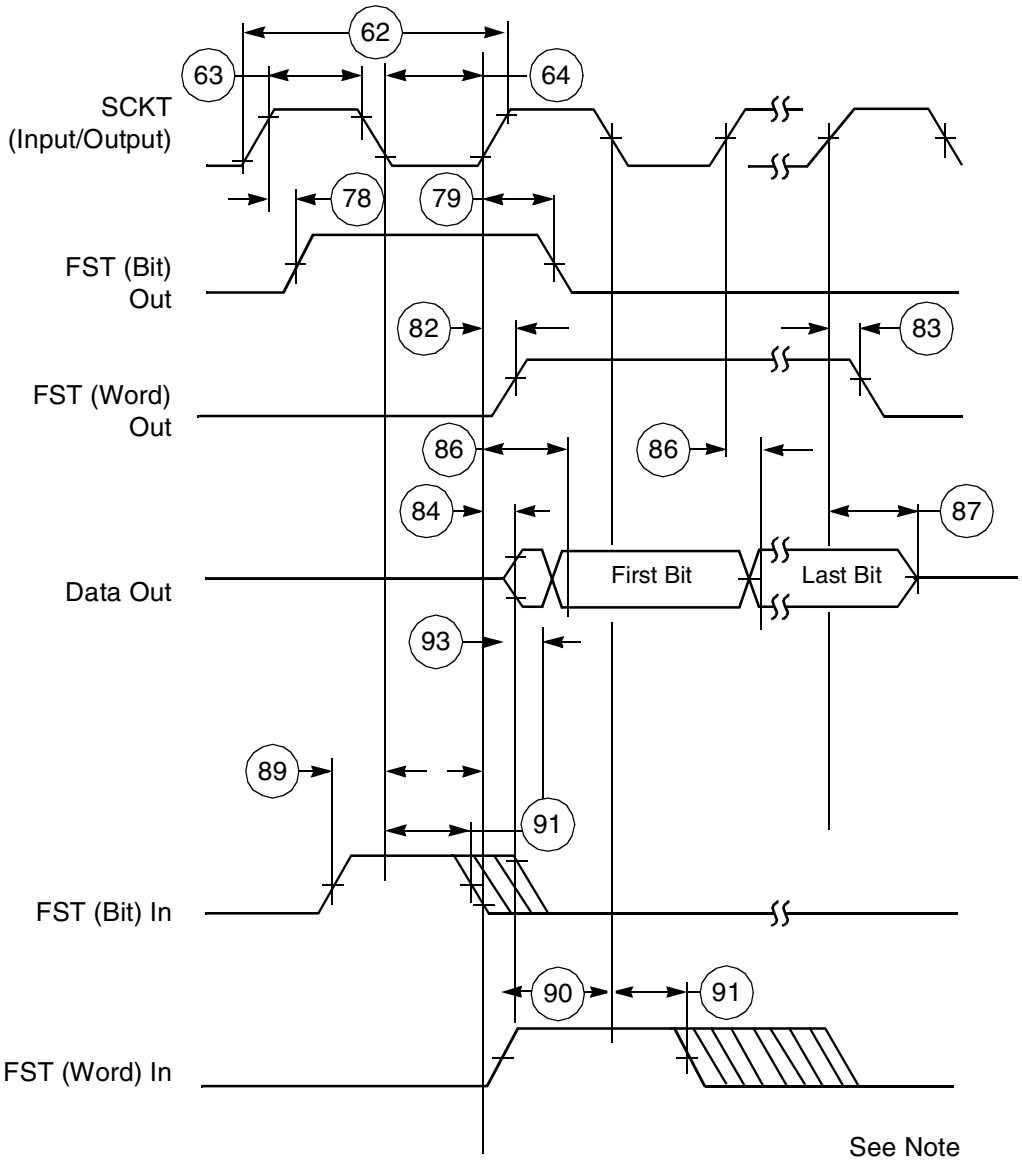
2 bl = bit length
wl = word length
wr = word length relative

3 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 25. ESAI Transmitter Timing

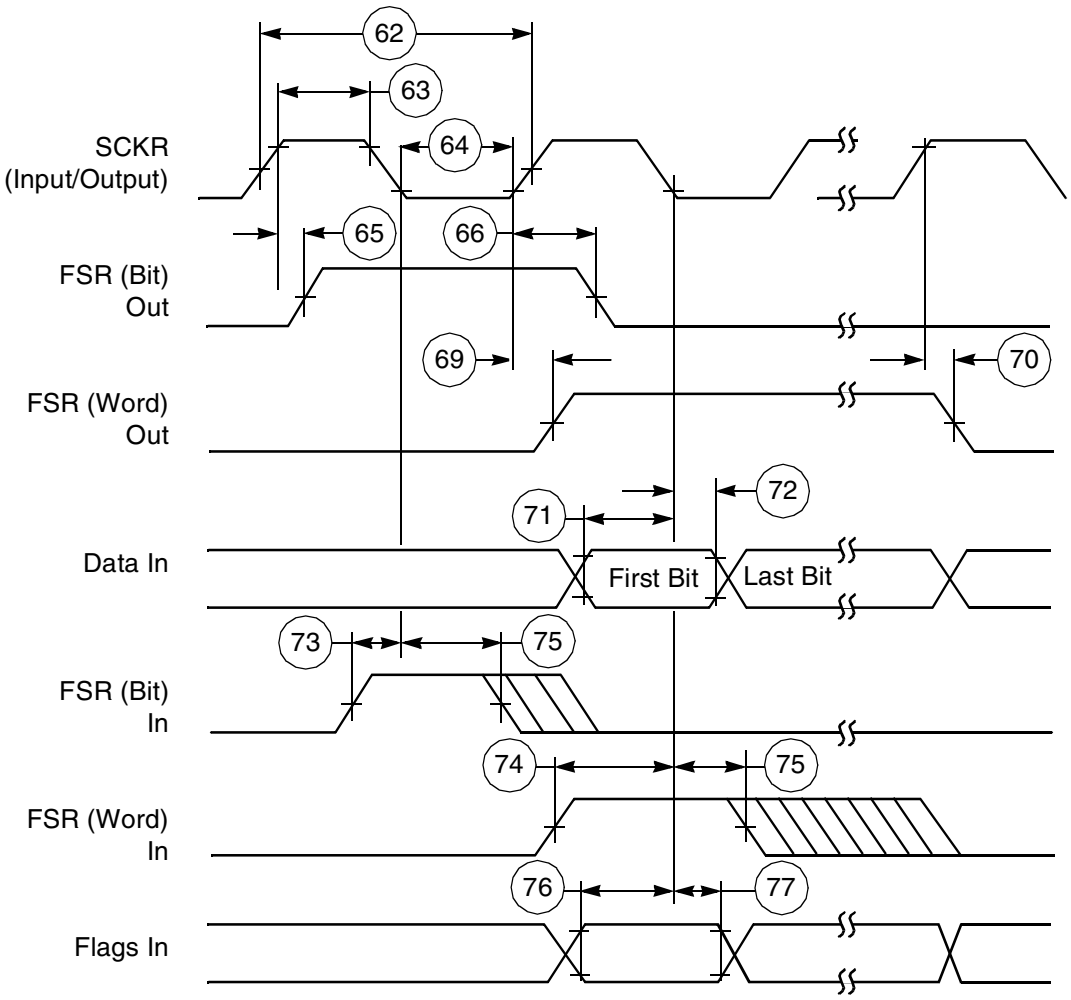


Figure 26. ESAI Receiver Timing

4.7.7 eSDHCv2 AC Electrical Specifications

Figure 27 depicts the timing of eSDHCv2, and Table 38 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 38:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

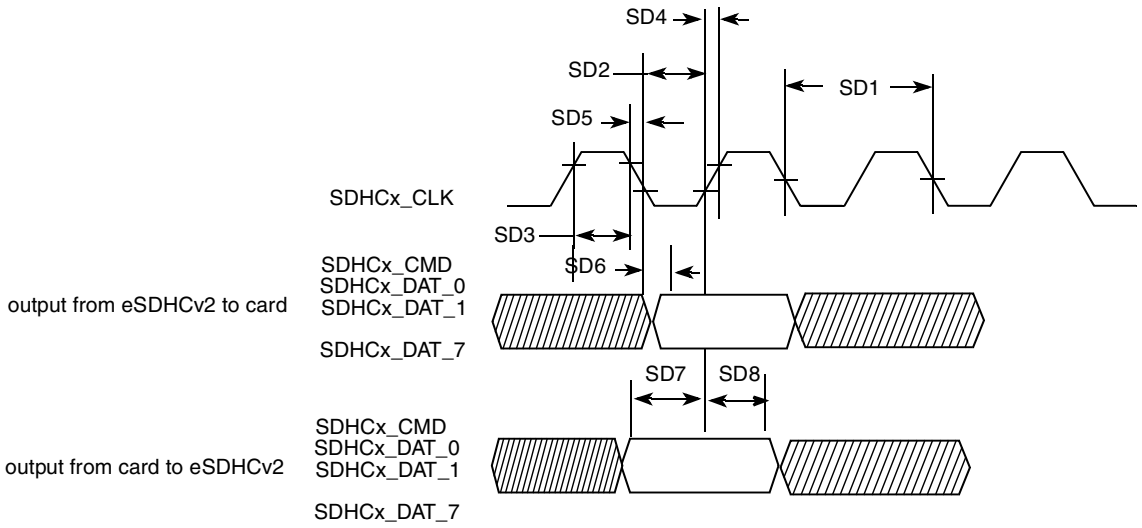


Figure 27. eSDHCv2 Timing

Table 38. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

1 In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.8 Fast Ethernet Controller (FEC) AC Electrical Specifications

This section describes the electrical information of the FEC module. The FEC is designed to support both 10- and 100-Mbps Ethernet networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps Media Independent Interface (MII) using a total of 18 pins. The 10-Mbps 7-wire interface that is restricted to a 10-Mbps data rate uses seven of the MII pins for connection to an external Ethernet transceiver.

4.7.8.1 FEC AC Timing

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.7.8.2 MII Receive Signal Timing

The MII receive timing signals consist of FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 39 lists MII receive channel timings.

Table 39. MII Receive Signal Timing

Num.	Characteristic[1]	Min.	Max.	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

[1] FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 28 shows the MII receive signal timings listed in Table 39.

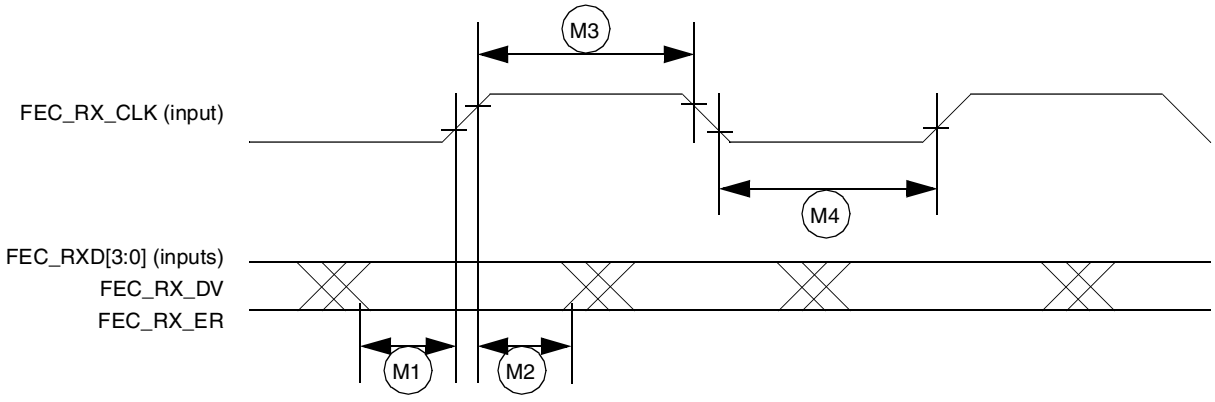


Figure 28. MII Receive Signal Timing Diagram

4.7.8.3 MII Transmit Signal Timing

The transmitter timing signals consist of FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency. Table 40 lists MII transmit channel timings.

Table 40. MII Transmit Signal Timing

Num	Characteristic[1]	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 29 shows the MII transmit signal timings listed in Table 40.

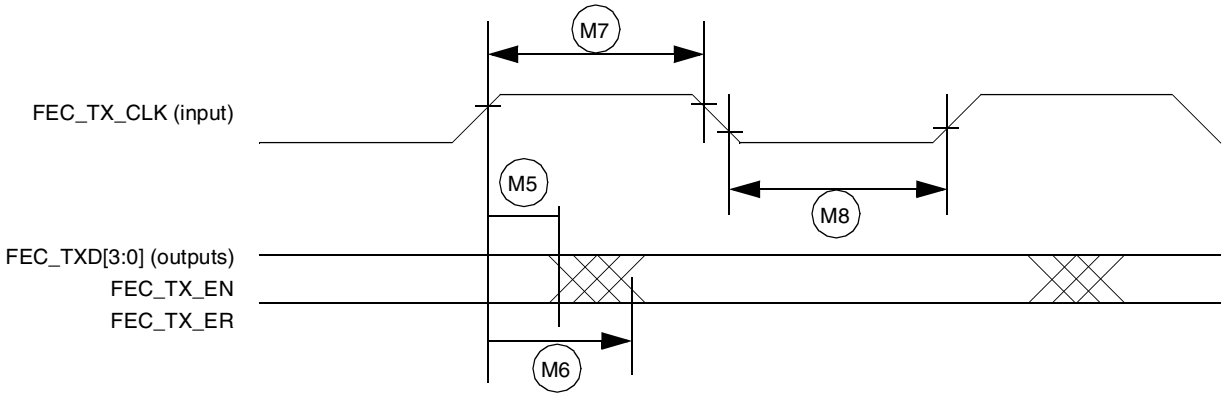


Figure 29. MII Transmit Signal Timing Diagram

4.7.8.4 MII Asynchronous Inputs Signal Timing

The MII asynchronous timing signals are FEC_CRS and FEC_COL. Table 41 lists MII asynchronous inputs signal timing.

Table 41. MII Asynch Inputs Signal Timing

Num	Characteristic	Min.	Max.	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

Figure 30 shows MII asynchronous input timings listed in Table 41.

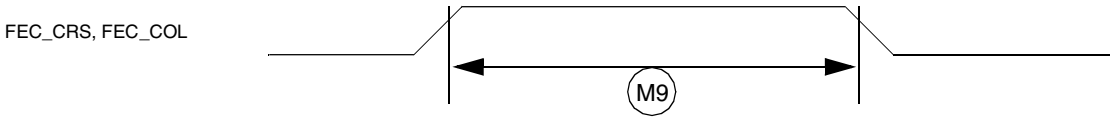


Figure 30. MII Asynch Inputs Timing Diagram

4.7.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 42 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 42. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 31 shows MII serial management channel timings listed in Table 42.

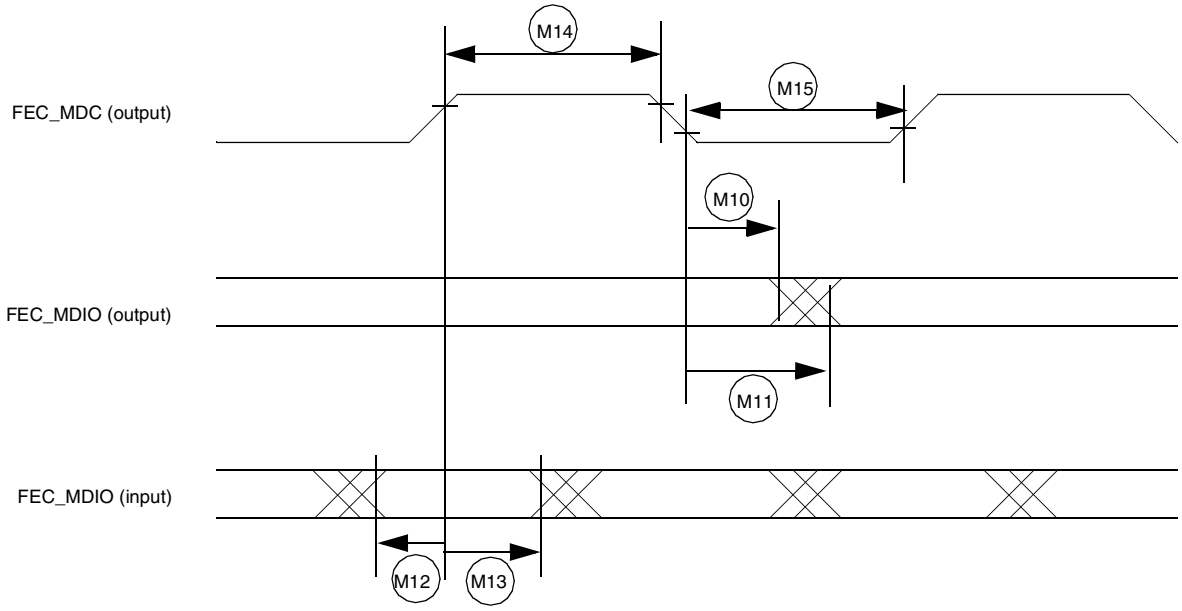


Figure 31. MII Serial Management Channel Timing Diagram

4.7.9 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) defined by IrDA® (Infrared Data Association). Refer to the IrDA® website for details on FIR and MIR protocols.

4.7.10 FlexCAN Module AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver outside the chip. For use in an application, the MAX3051 is recommended. For details, please refer to the MAX3051 datasheetThe MCIMX35 has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pads. Refer to the IOMUX chapter of the *MCIMX35 Multimedia Applications Processor Reference Manual* to see which pads expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.7.11 I^2C AC Electrical Specifications

This section describes the electrical characteristics of the I^2C module.

4.7.11.1 I²C Module Timing

Figure 32 depicts the timing of the I²C module. Table 43 lists the I²C module timing parameters.

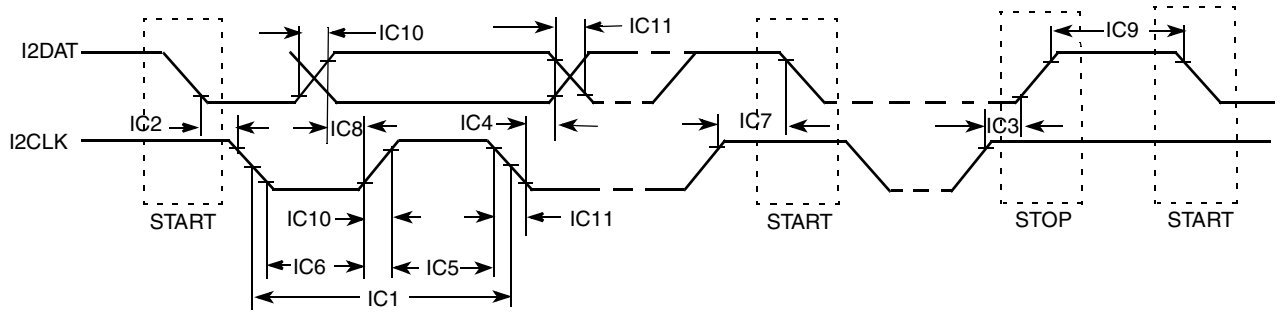


Figure 32. I²C Bus Timing Diagram

Table 43. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	—	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	—	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for the I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

3 A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4.7.12 IPU—Sensor Interfaces

4.7.12.1 Supported Camera Sensors

Table 44 lists the known supported camera sensors at the time of publication.

Table 44. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI-SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630, OV2640
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors have not been validated at the time of publication.

4.7.12.2 Functional Description

There are three timing modes supported by the IPU.

4.7.12.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which typically include image processing capability, support video mode transfer operations. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of the ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with an EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

4.7.12.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 33.

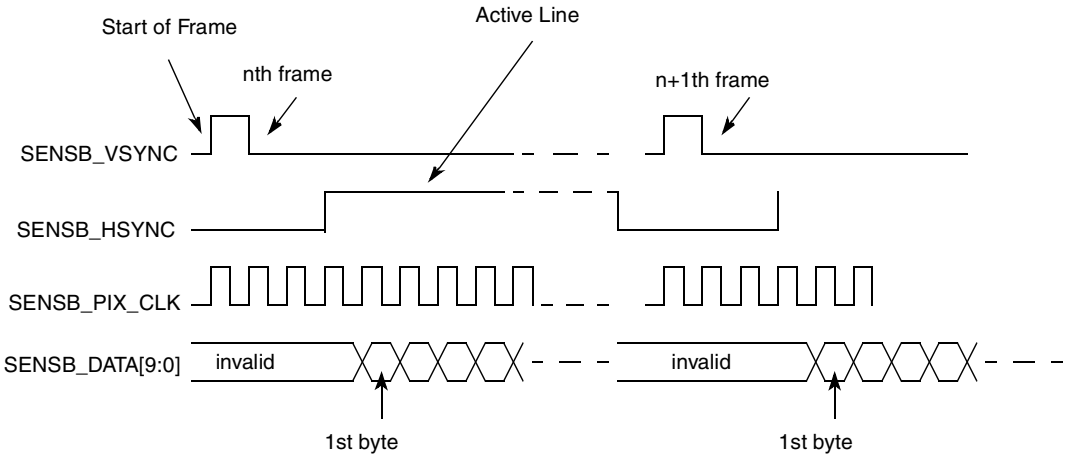


Figure 33. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timing corresponds to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. The pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of the line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the SENSB_HSYNC timing repeats. For the next frame, the SENSB_VSYNC timing repeats.

4.7.12.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.7.12.2.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 34. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

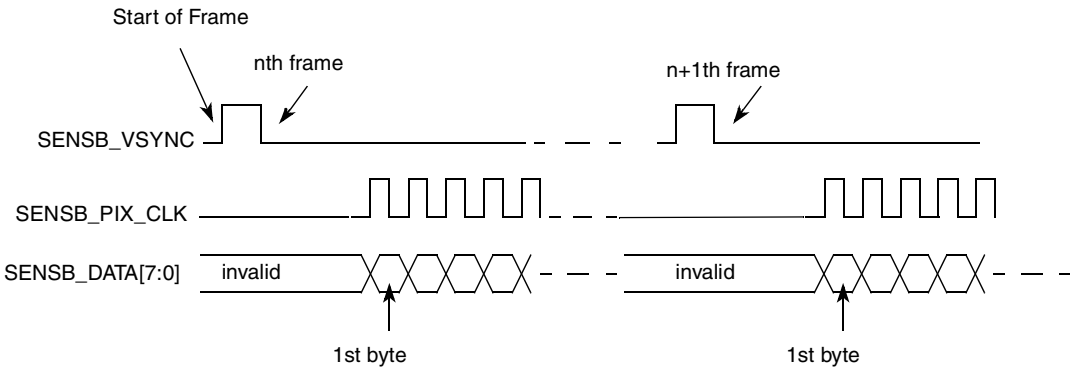


Figure 34. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 34 is that of a Motorola sensor. Some other sensors may have slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.7.12.3 Electrical Characteristics

Figure 35 depicts the sensor interface timing, and Table 45 lists the timing parameters.

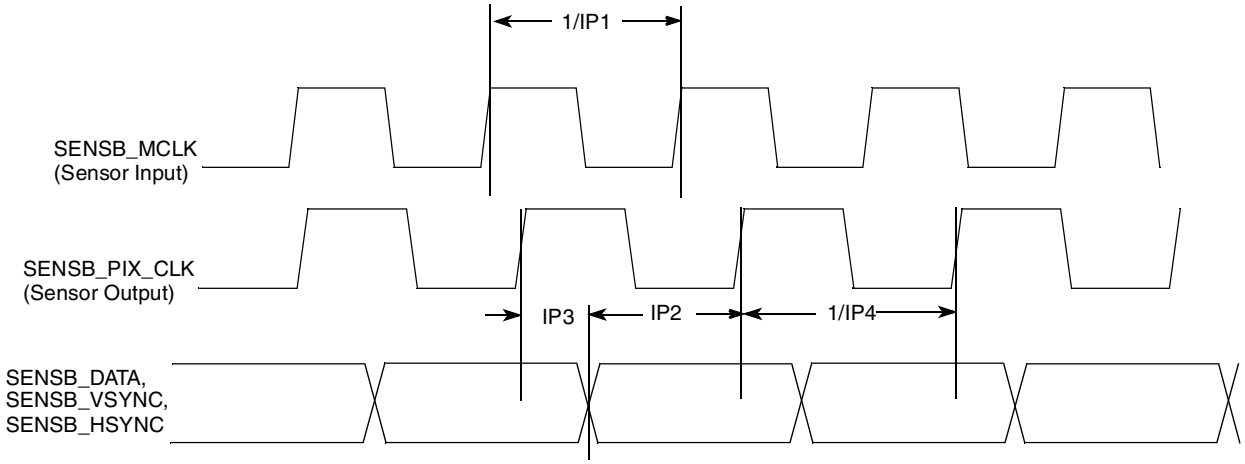


Figure 35. Sensor Interface Timing Diagram

Table 45. Sensor Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

4.7.13 IPU–Display Interfaces

4.7.13.1 Synchronous Interfaces

4.7.13.1.4 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 36 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is as follows:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted to the display. When disabled, the data is invalid and the trace is off.

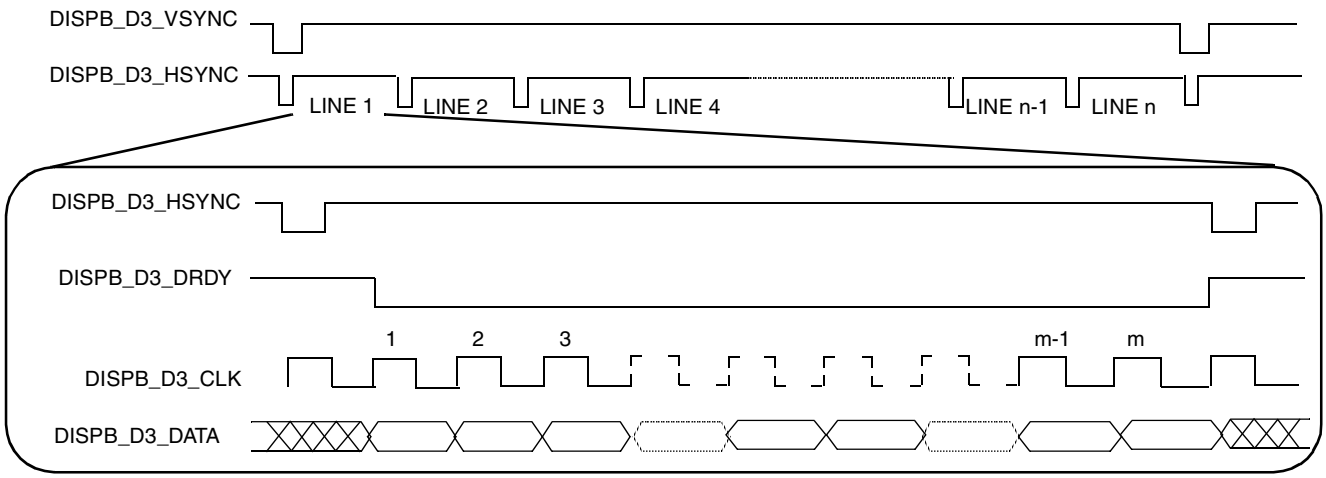


Figure 36. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.13.1.5 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 37 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

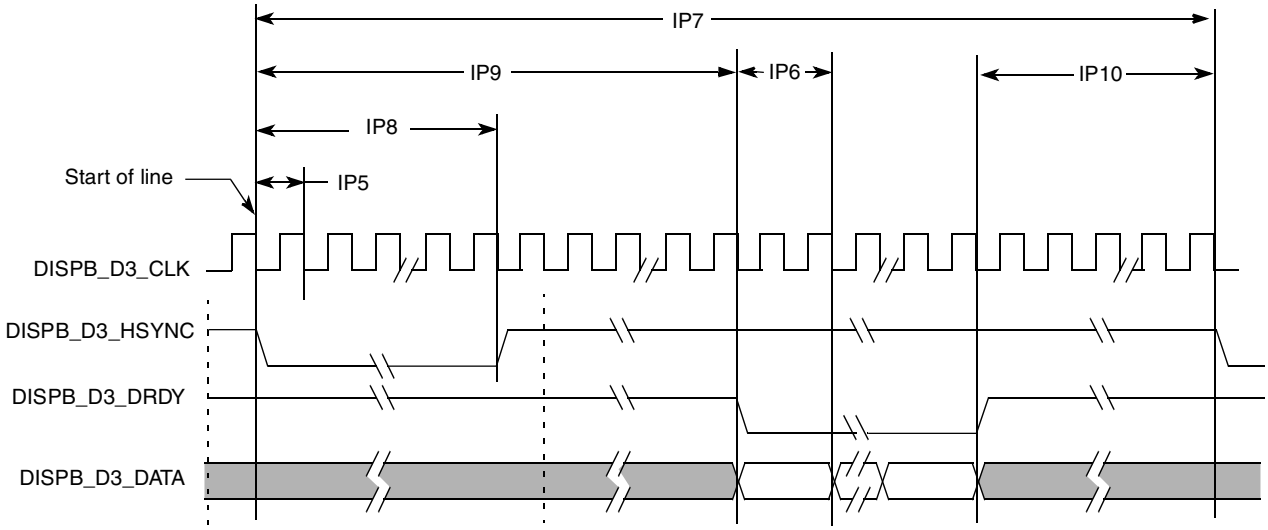


Figure 37. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 38 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

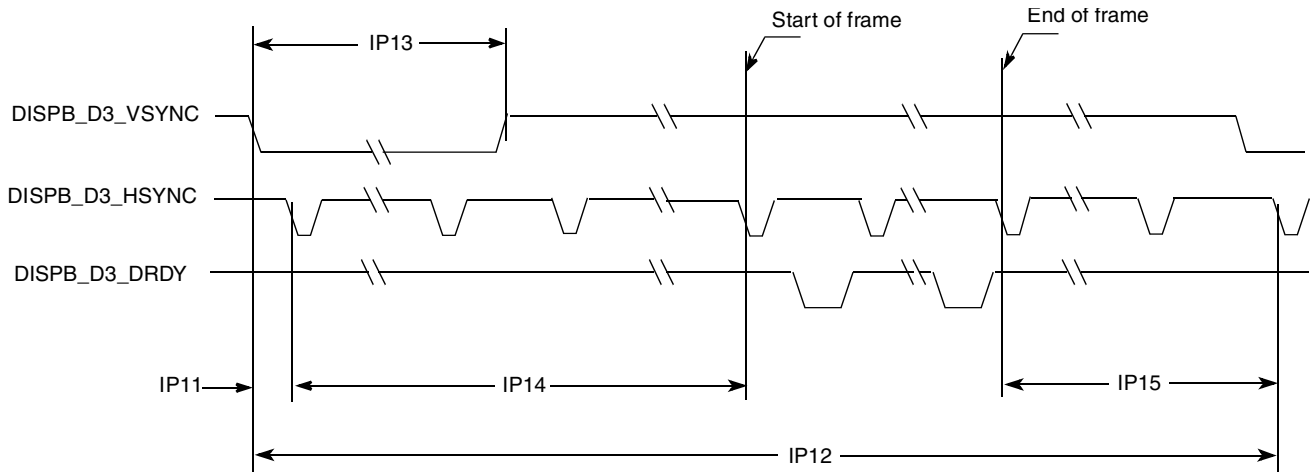


Figure 38. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 46 shows timing parameters of signals presented in Figure 37 and Figure 38.

Table 46. Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	Tdicp[1]	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D+1) * Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH+1) * Tdpcp	ns
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH+1) * Tdpcp	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP * Tdpcp	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH–BGXP–FW) * Tdpcp	ns
IP11	HSYNC delay	Thsd	H_SYNC_DELAY * Tdpcp	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT+1) * Tsw	ns
IP13	VSYNC width	Tvsw	if V_SYNC_WIDTH_L = 0 than (V_SYNC_WIDTH+1) * Tdpcp else (V_SYNC_WIDTH+1) * Tsw	ns

Table 46. Synchronous Display Interface Timing Parameters—Pixel Level (continued)

ID	Parameter	Symbol	Value	Units
IP14	Vertical blank interval 1	Tvbi1	BGYP * Tsw	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) * Tsw	ns

1 Display interface clock period immediate value

Display interface clock period average value.

$$\overline{T}dicp = T_{HSP\_CLK} \cdot \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}$$

Figure 39 depicts the synchronous display interface timing for access level, and Table 47 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

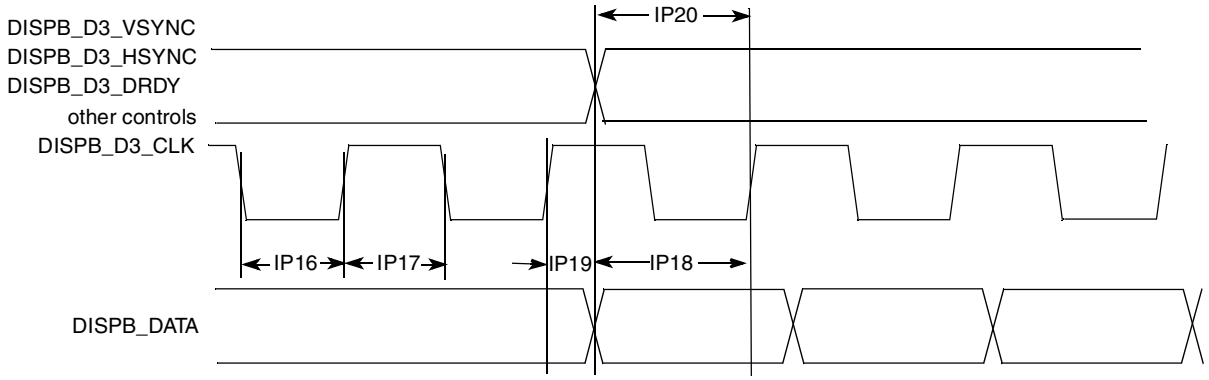


Figure 39. Synchronous Display Interface Timing Diagram—Access Level

Table 47. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.5	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.5	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd-3.5	Tdicu	—	ns

Table 47. Synchronous Display Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-3.5	Tdicp-Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd-3.5	Tdicu	—	ns

1 The exact conditions not have been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

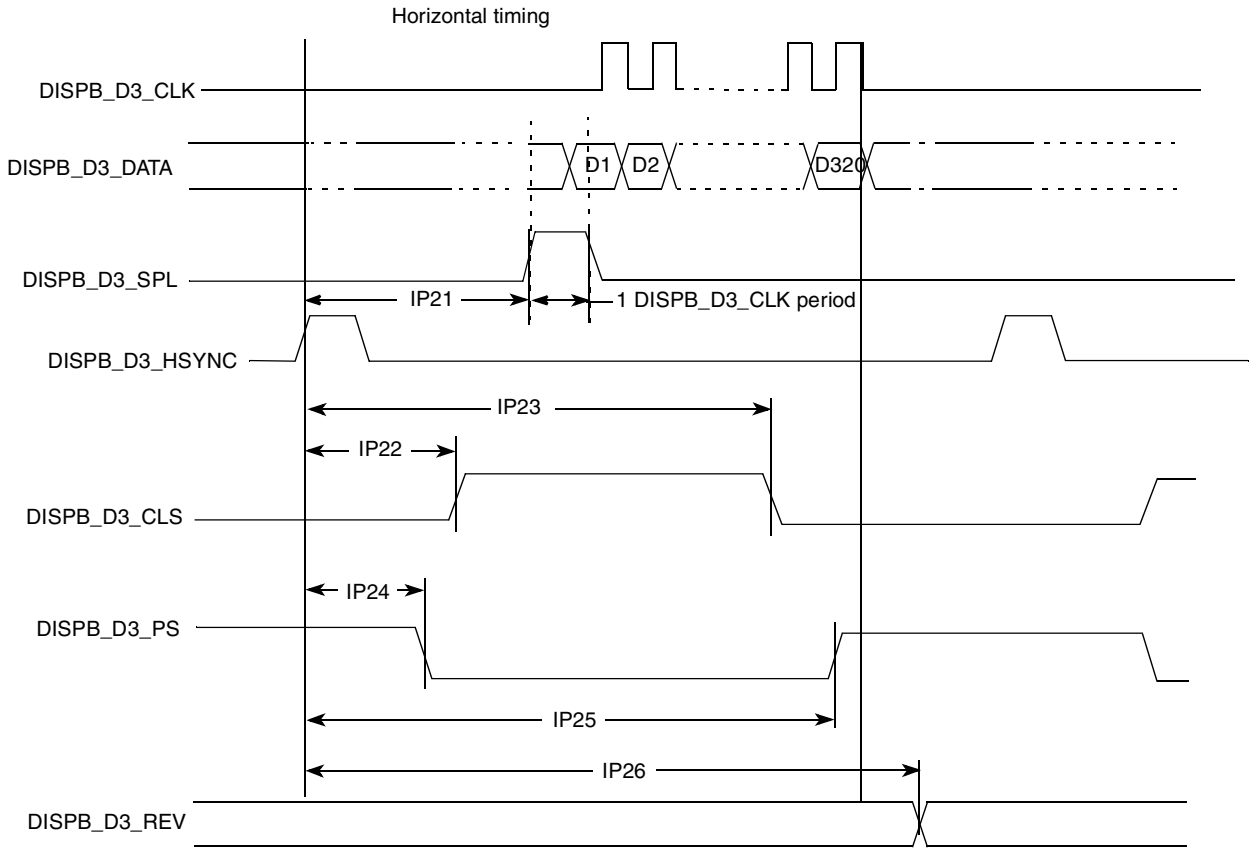
3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.7.13.2 Interface to Sharp HR-TFT Panels

Figure 40 depicts the Sharp HR-TFT panel interface timing, and Table 48 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to Section 4.7.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.” The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW+1=320 pixel/line, FH+1=240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 40. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 48. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) * Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY * Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY * Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY * Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY * Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY * Tdpcp	ns

4.7.13.3 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.7.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.7.13.3.6 Interface to a TV Encoder—Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 41 depicts the interface timing.

- The frequency of the clock DISPB_D3_CLK is 27 MHz.
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
  - At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
  - At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

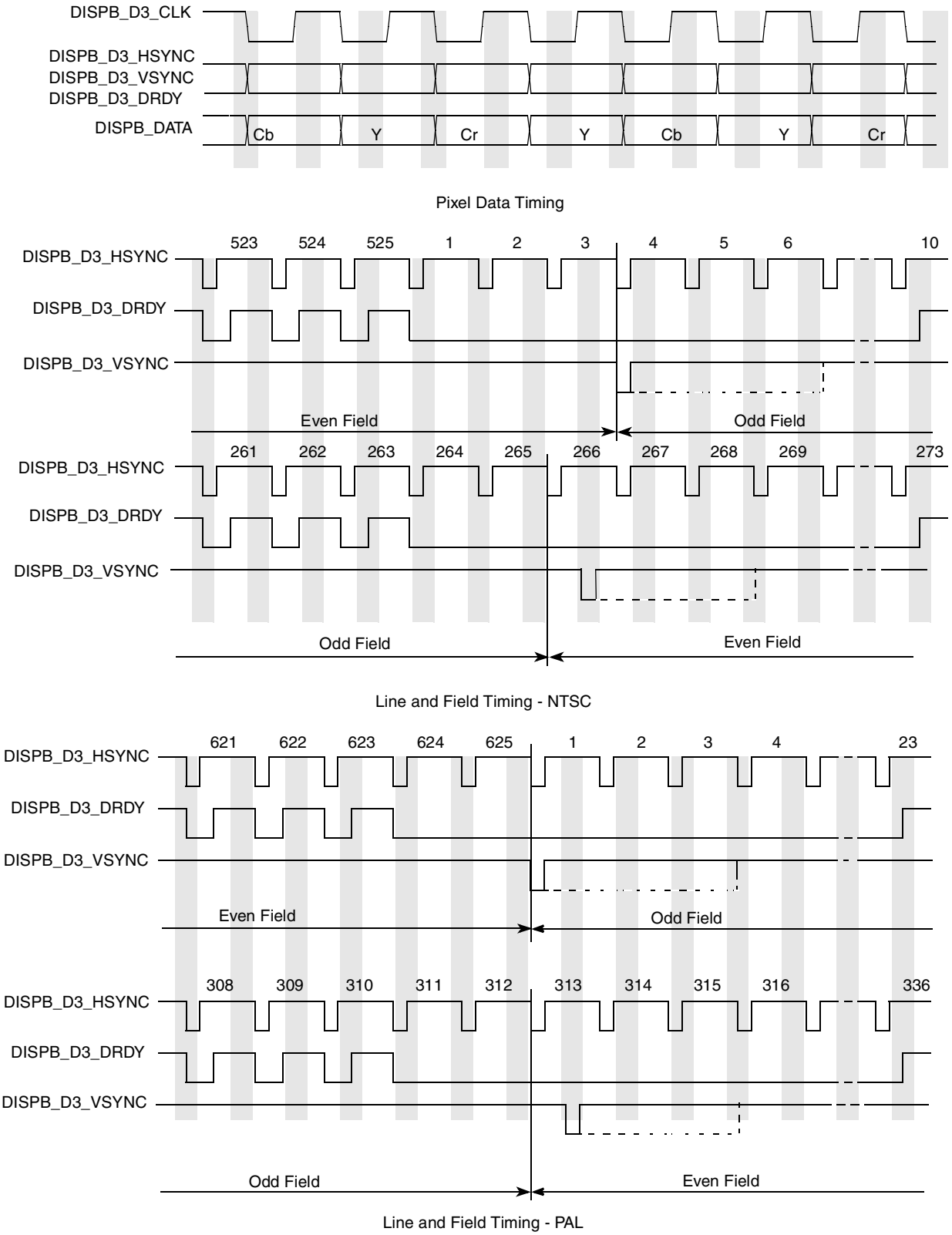


Figure 41. TV Encoder Interface Timing Diagram

4.7.13.3.7 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.7.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.7.13.4 Asynchronous Interfaces

4.7.13.4.8 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - — Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - — Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - — Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - — Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock—The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) or by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals change only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k), and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK—In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode—In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according to the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 42, Figure 43, Figure 44, and Figure 45. These timing images correspond to active-low DISPB_D*n*_CS, DISPB_D*n*_WR and DISPB_D*n*_RD signals.

Additionally, the IPU allows a programmable pause between two bursts. The pause is defined in the HSP_CLK cycles. It allows the prevention of timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

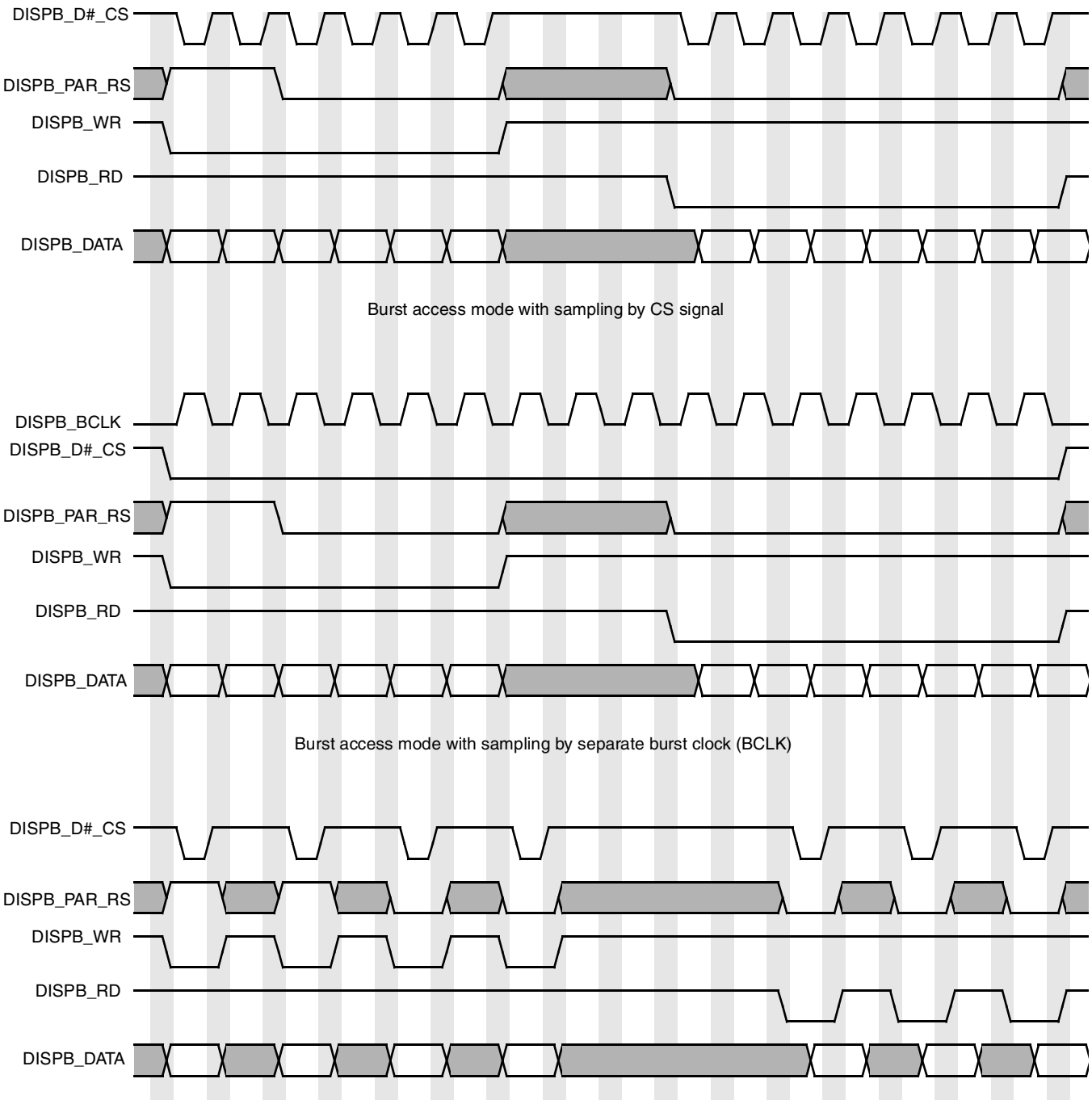


Figure 42. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram

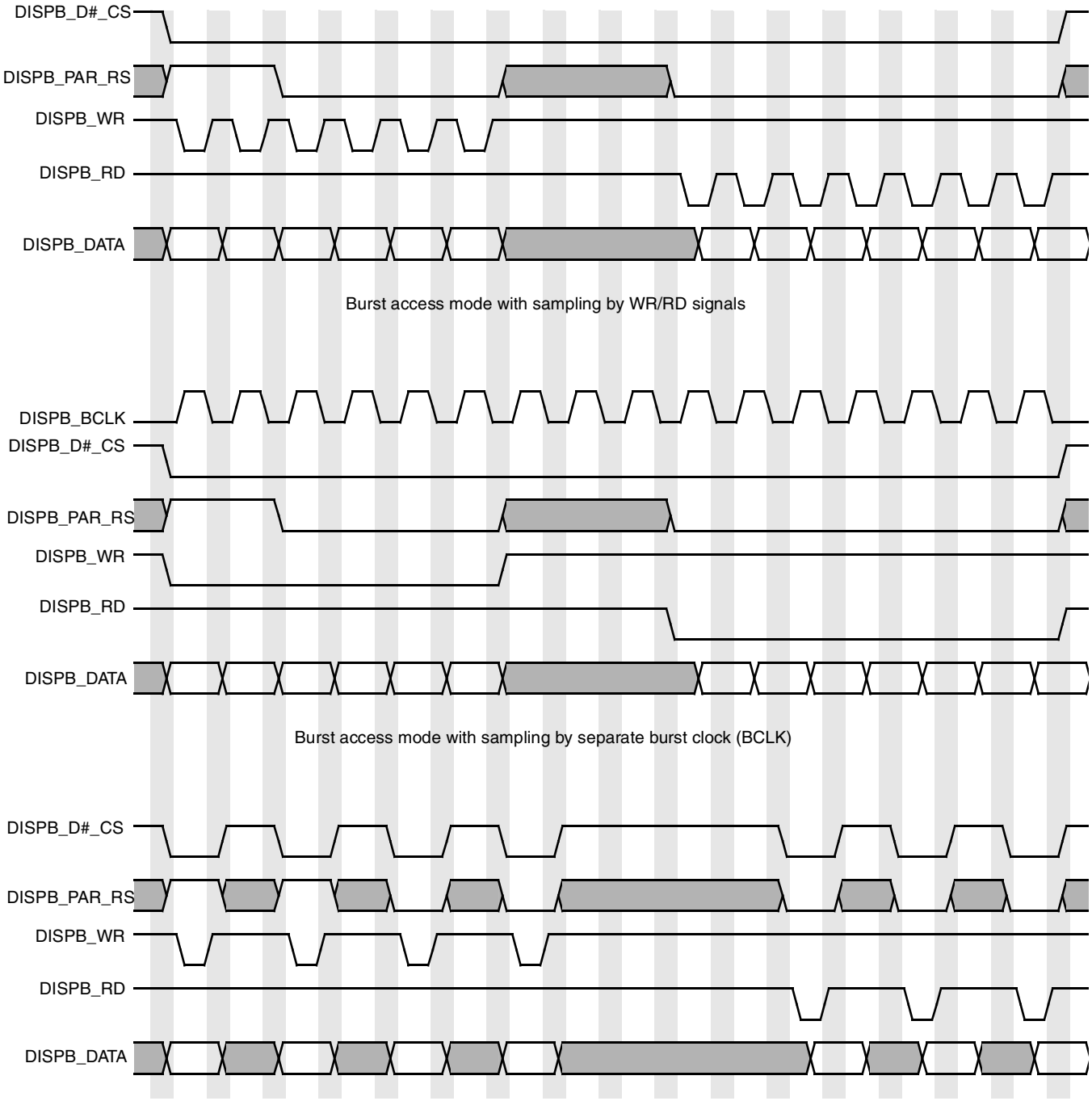
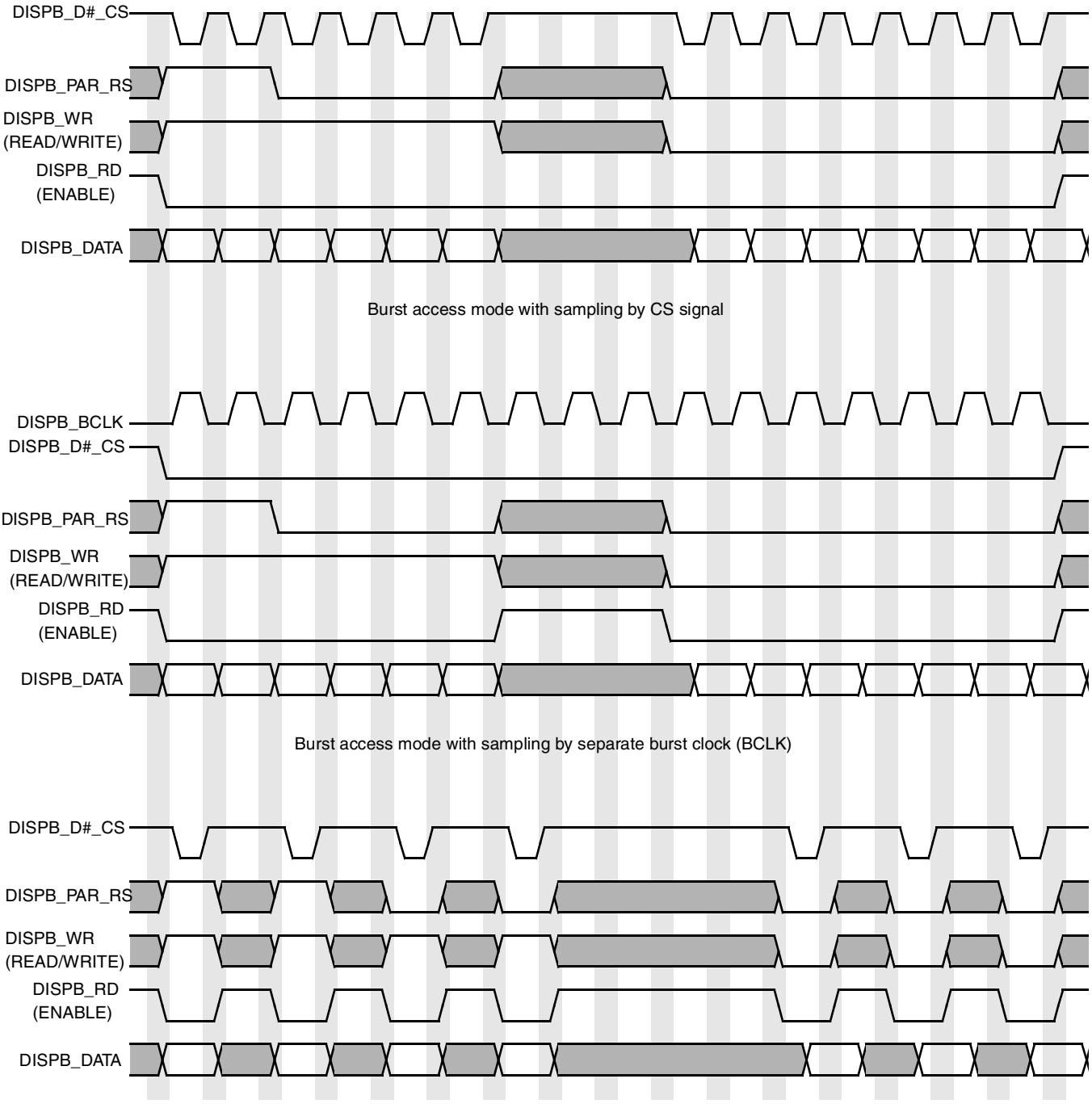


Figure 43. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram



Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 44. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

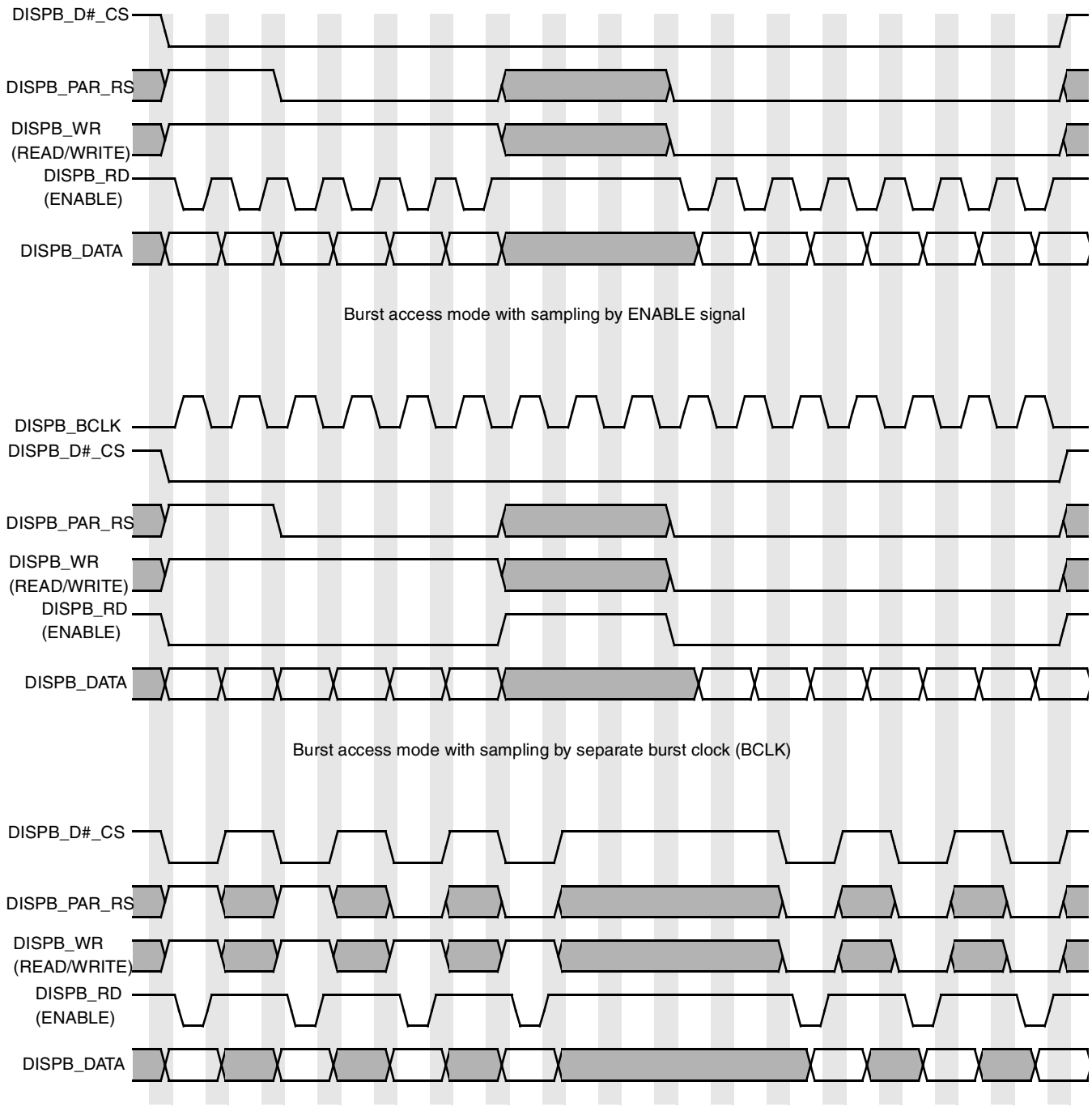


Figure 45. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the

DI_DISP*n*_TIME_CONF_3 registers (*n* = 0,1,2). Figure 46 shows timing of the parallel interface with read wait states.

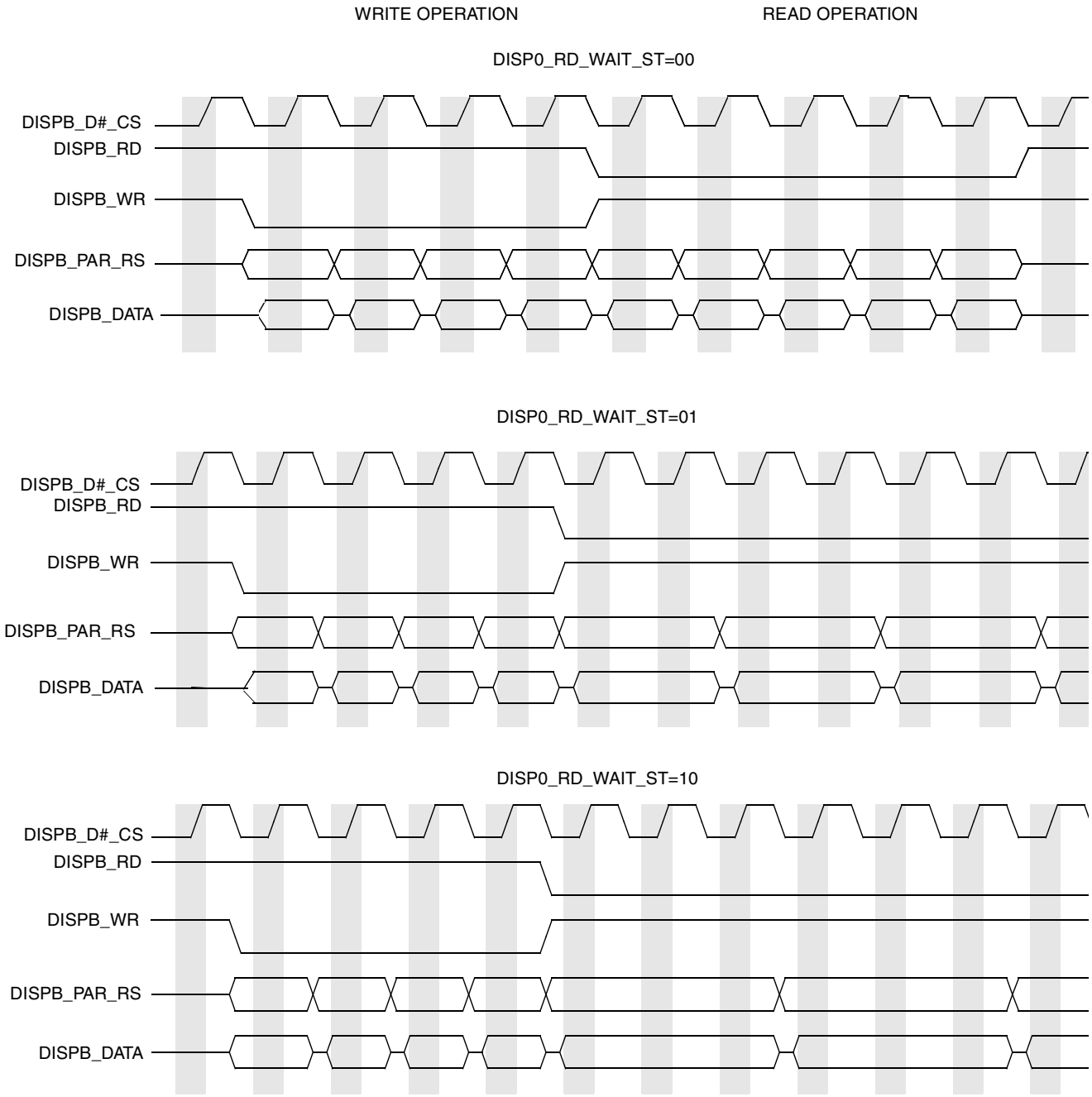


Figure 46. Parallel Interface Timing Diagram—Read Wait States

4.7.13.4.9 Parallel Interfaces, Electrical Characteristics

Figure 47, Figure 49, Figure 48, and Figure 50 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 49 lists the timing parameters at display access level. All

timing images are based on active low control signals (signal polarity is controlled via the DI_DISP_SIG_POL register).

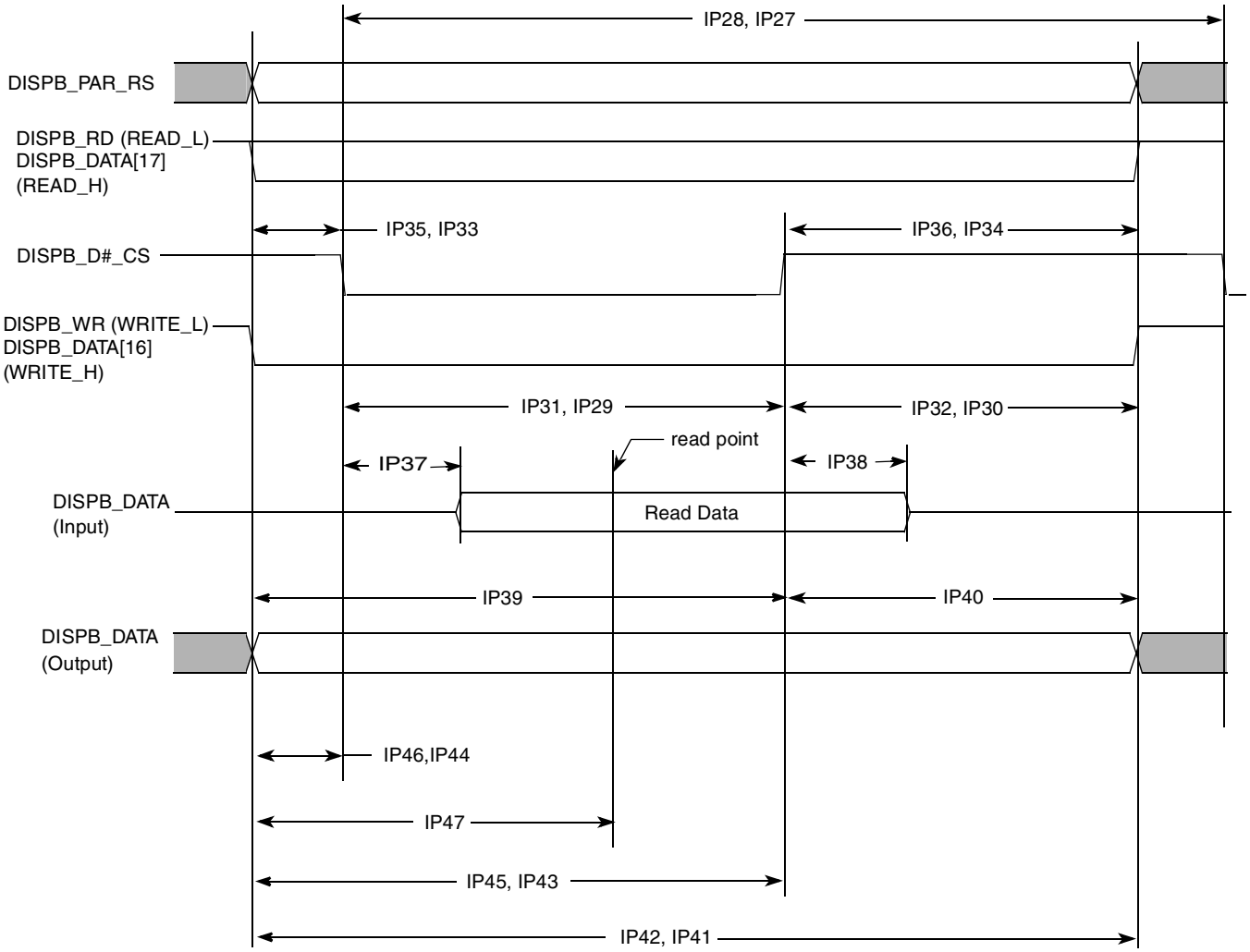


Figure 47. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

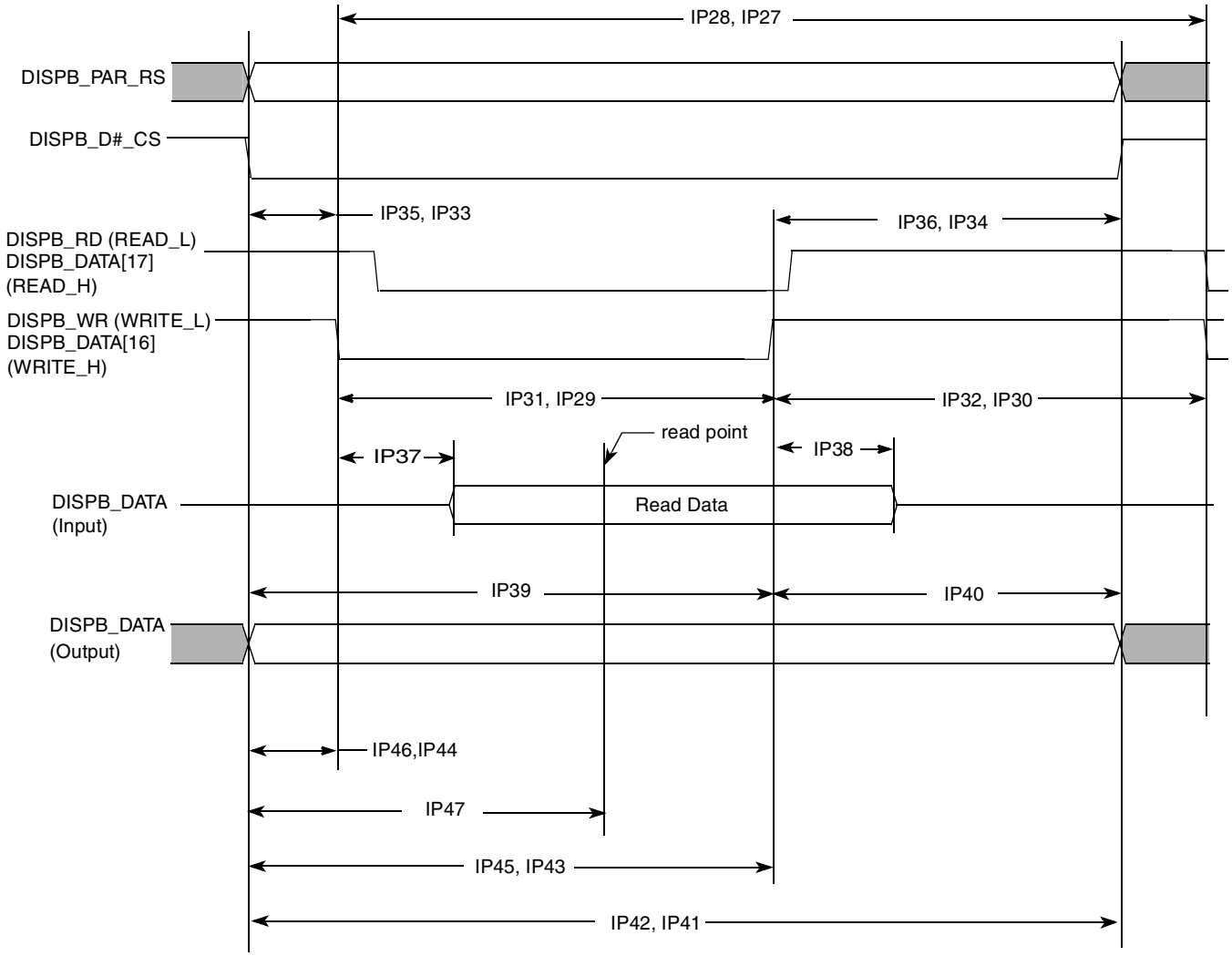


Figure 48. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

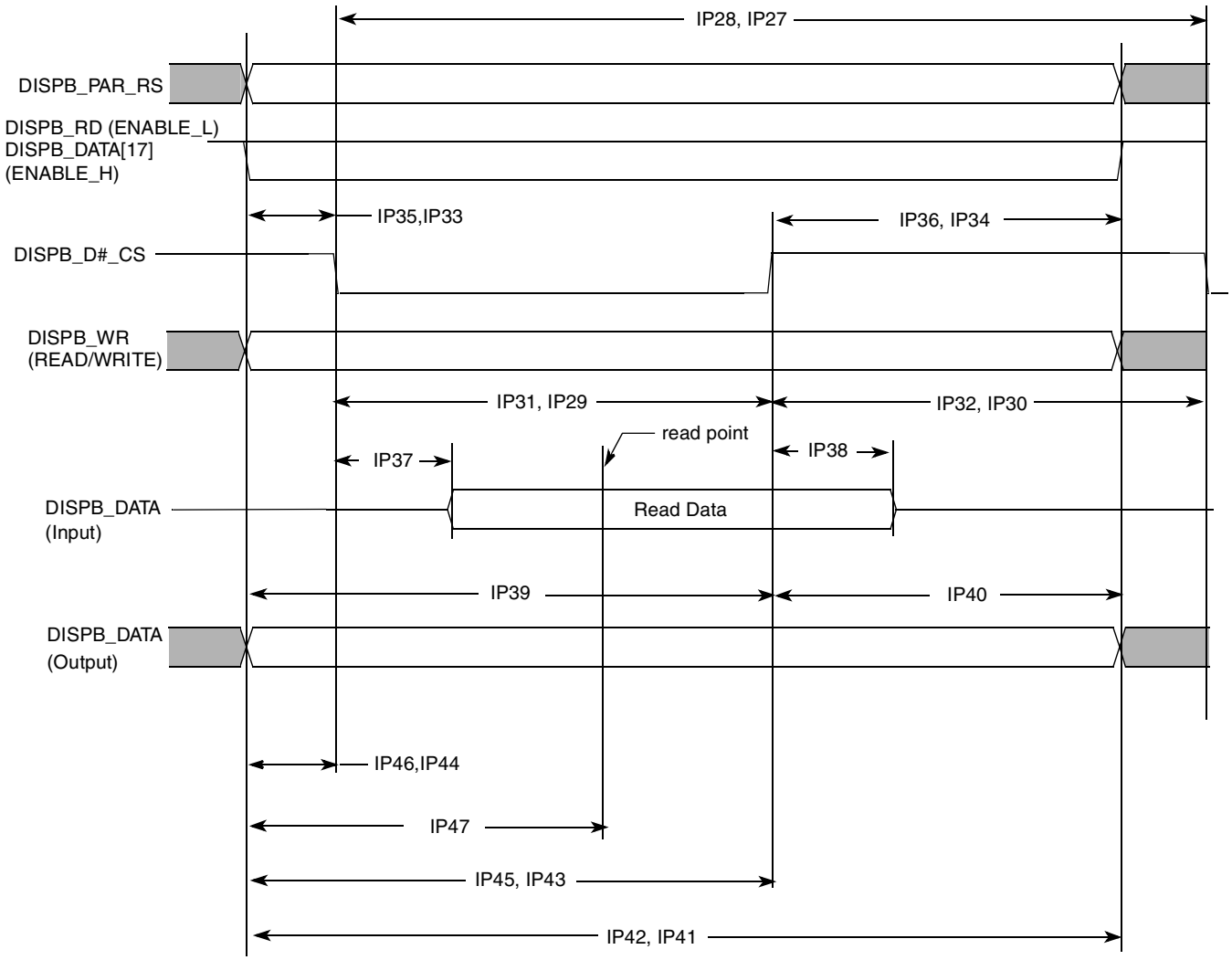


Figure 49. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

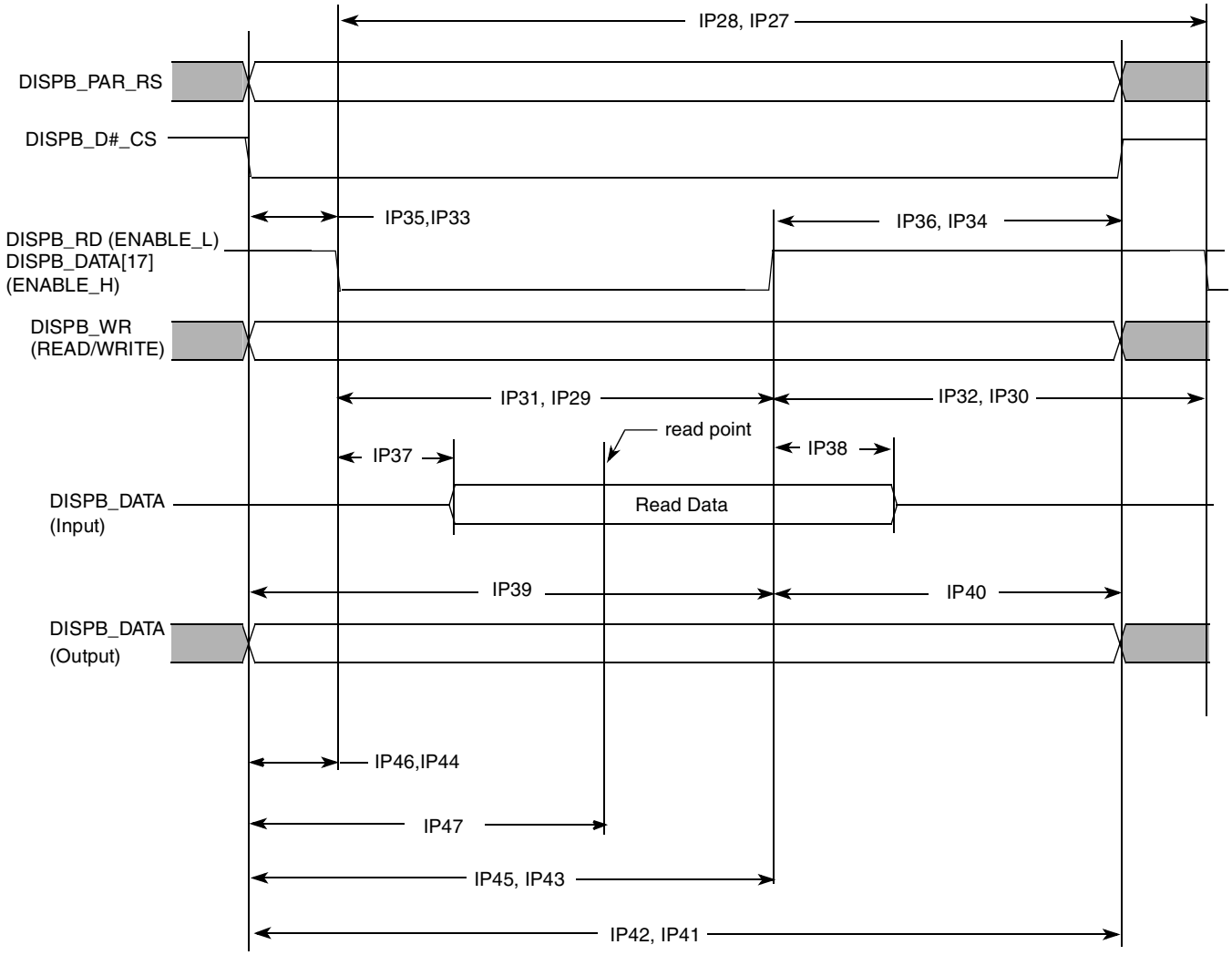


Figure 50. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 49. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr-1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw-1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP29	Read low pulse width	Trl	Tdicdr-Tdicur-1.5	Tdicdr[4]-Tdicur[5]	Tdicdr-Tdicur+1.5	ns
IP30	Read high pulse width	Trh	Tdicpr-Tdicdr+Tdicur-1.5	Tdicpr-Tdicdr+ Tdicur	Tdicpr-Tdicdr+Tdicur+1.5	ns
IP31	Write low pulse width	Twl	Tdicdw-Tdicuw-1.5	Tdicdw[6]-Tdicuw[7]	Tdicdw-Tdicuw+1.5	ns
IP32	Write high pulse width	Twh	Tdicpw-Tdicdw+ Tdicuw-1.5	Tdicpw-Tdicdw+ Tdicuw	Tdicpw-Tdicdw+ Tdicuw+1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur-1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr-Tdicdr-1.5	Tdicpr-Tdicdr	—	ns

Table 49. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP35	Controls setup time for write	Tdcsw	Tdicuw-1.5	Tdicuw	—	ns
IP36	Controls hold time for write	Tdchw	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns
IP37	Slave device data delay[8]	Tracc	0	—	Tdrp[9]-Tlbd[10]-Tdicur-1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp-Tlbd-Tdicdr+1.5	—	Tdicpr-Tdicdr-1.5	ns
IP39	Write data setup time	Tds	Tdicdw-1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns
IP41	Read period[2]	Tdicpr	Tdicpr-1.5	Tdicpr	Tdicpr+1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw-1.5	Tdicpw	Tdicpw+1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr-1.5	Tdicdr	Tdicdr+1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur-1.5	Tdicur	Tdicur+1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw-1.5	Tdicdw	Tdicdw+1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw-1.5	Tdicuw	Tdicuw+1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp-1.5	Tdrp	Tdrp+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device-specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.7.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 51 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux connects the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP*n*_CONF registers (*n* = 1,2).

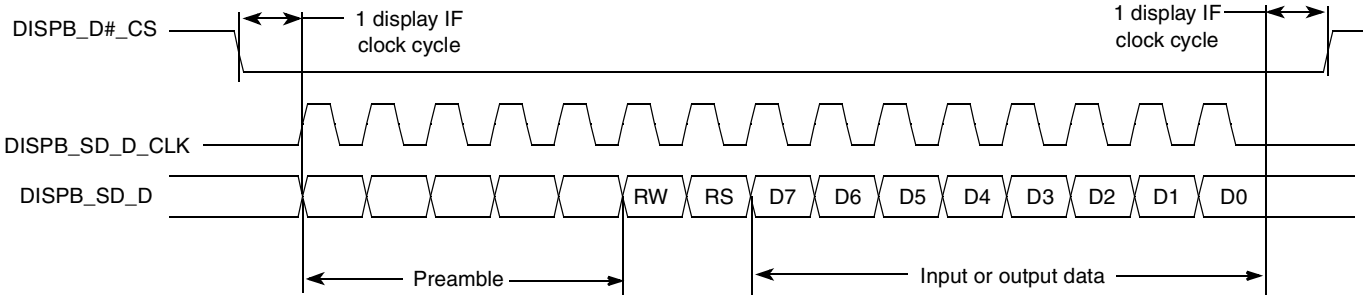


Figure 51. 3-Wire Serial Interface Timing Diagram

Figure 52 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

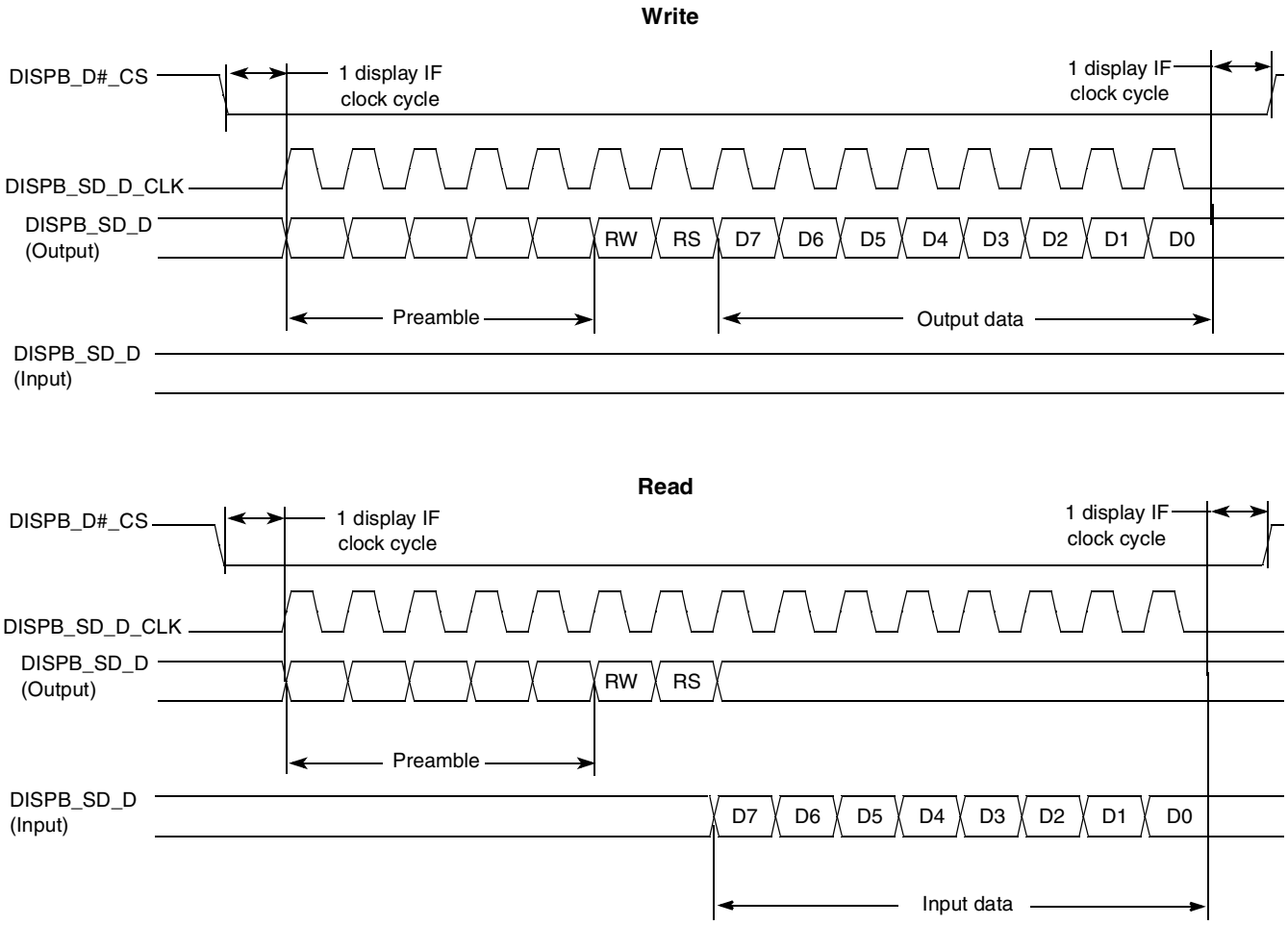


Figure 52. 4-Wire Serial Interface Timing Diagram

Figure 53 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

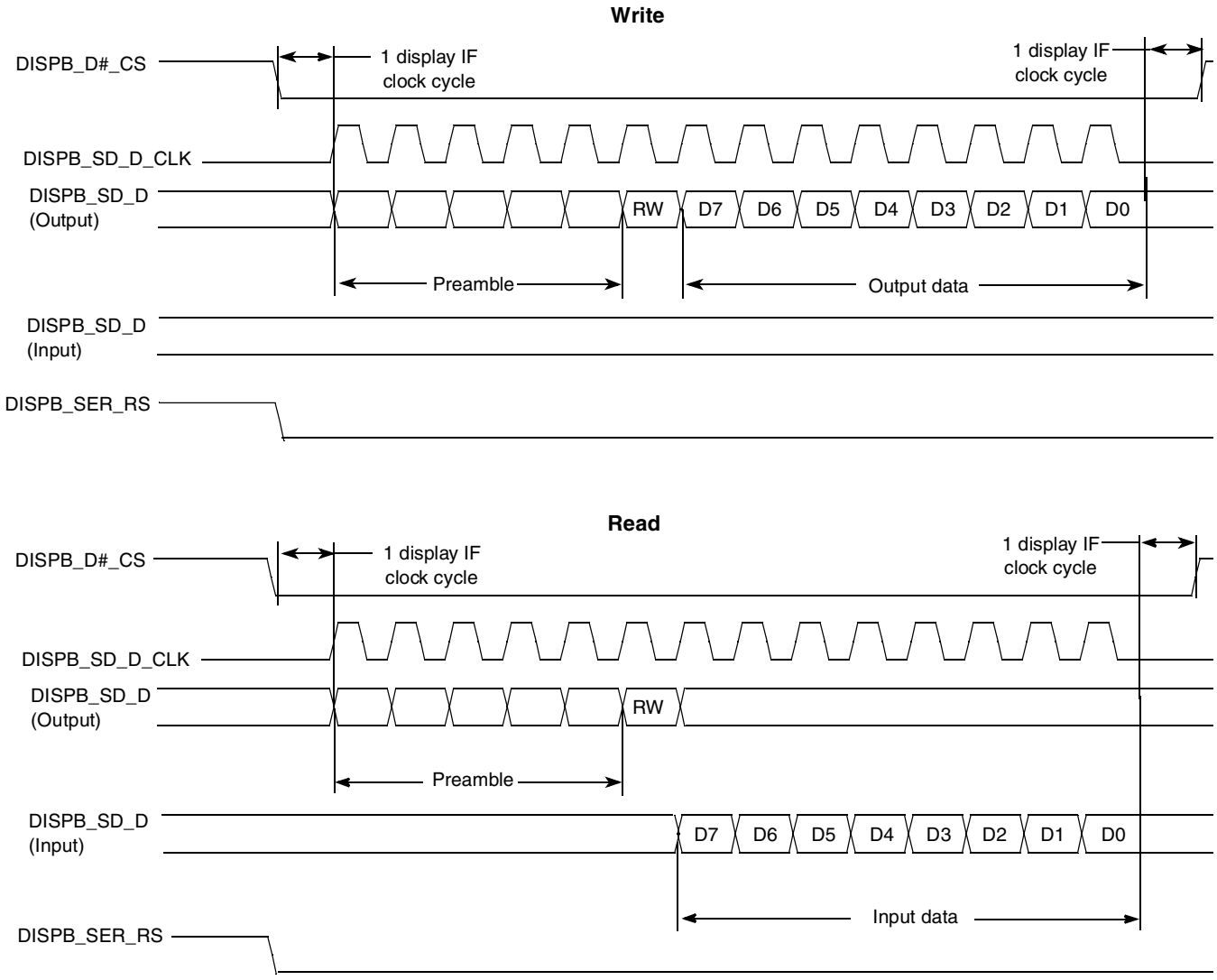


Figure 53. 5-Wire Serial Interface (Type 1) Timing Diagram

Figure 54 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

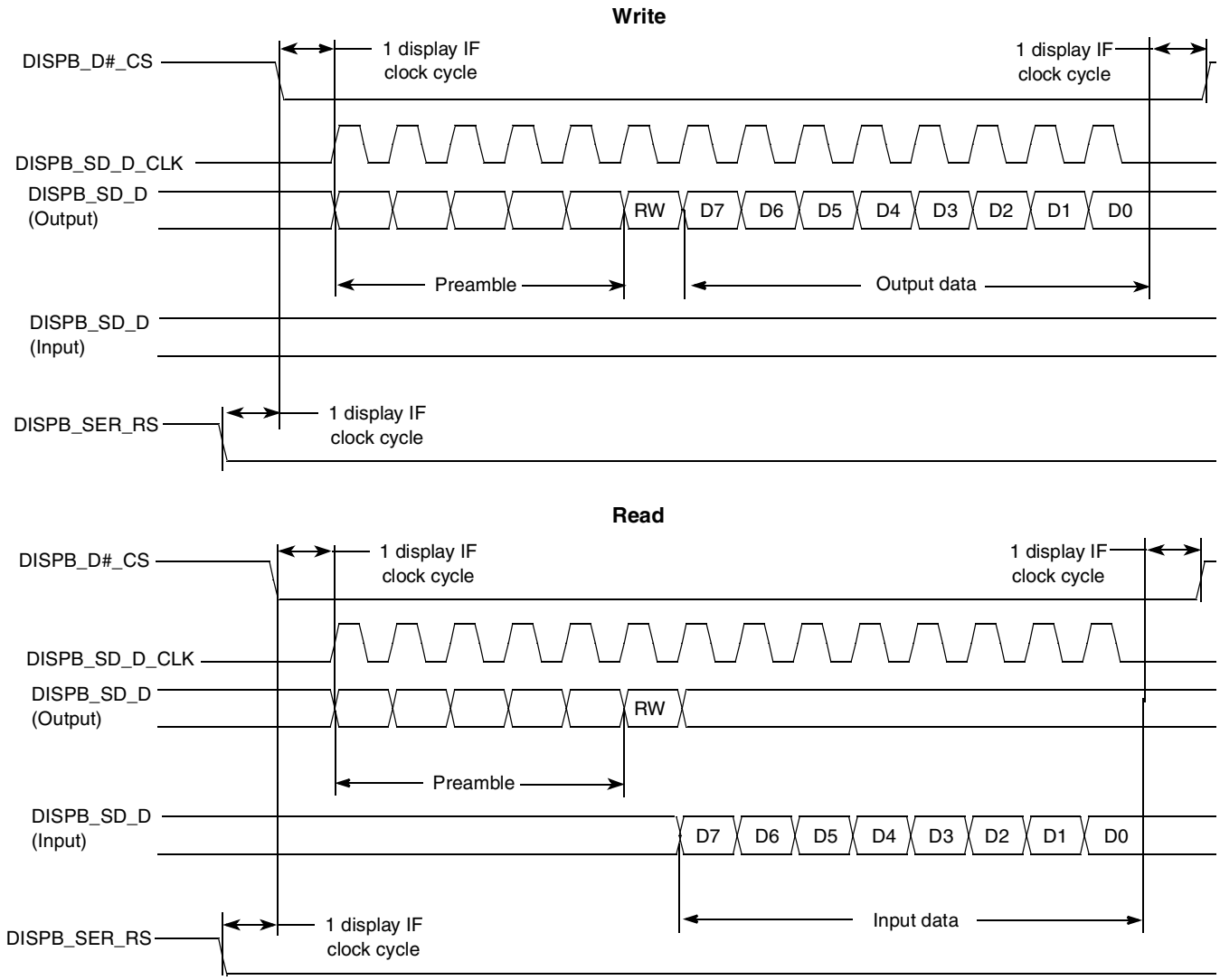


Figure 54. 5-Wire Serial Interface (Type 2) Timing Diagram

4.7.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 55 depicts timing of the serial interface. Table 50 lists the timing parameters at display access level.

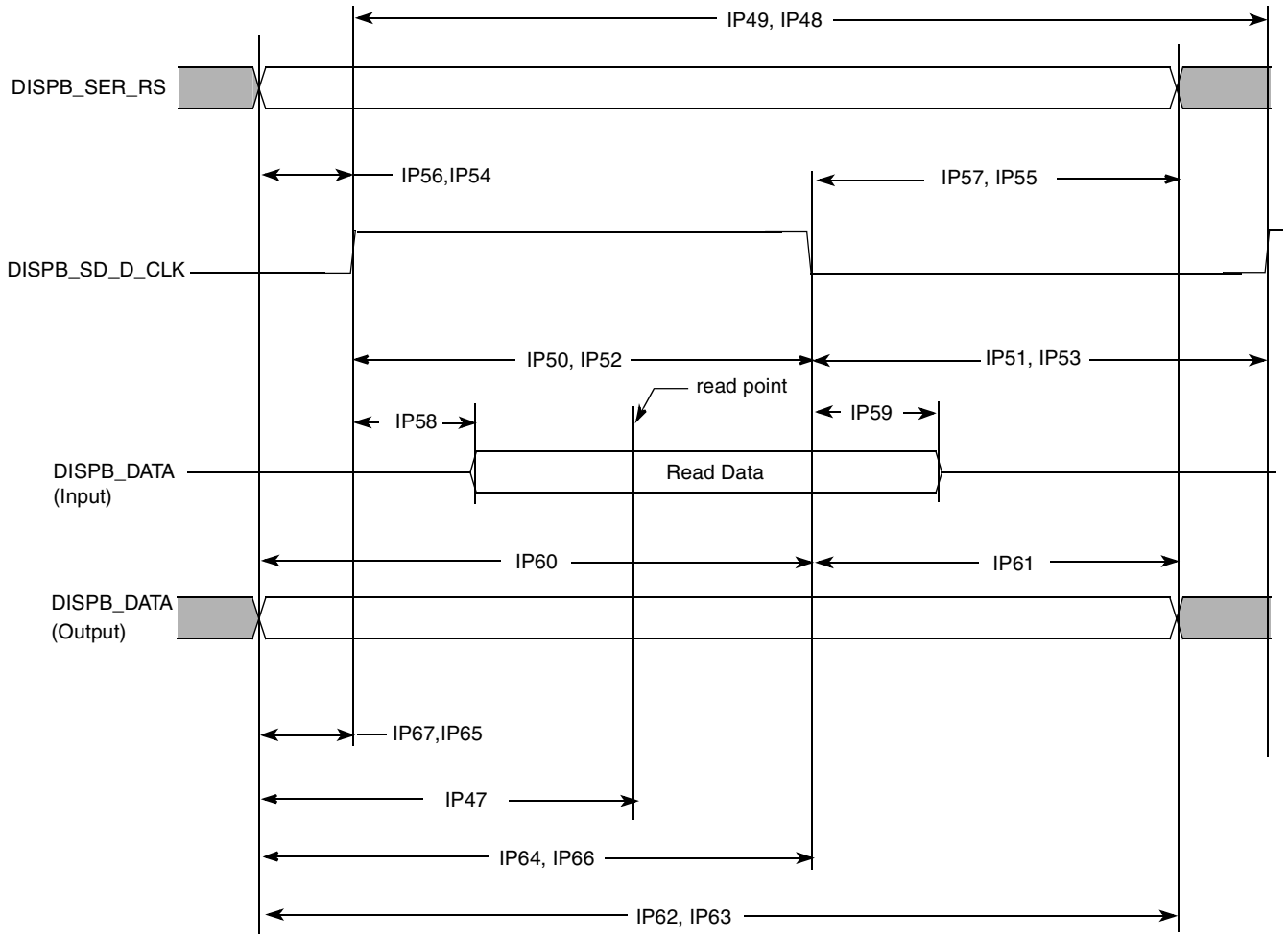


Figure 55. Asynchronous Serial Interface Timing Diagram

Table 50. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr-1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw-1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr-Tdicur-1.5	Tdicdr[4]-Tdicur[5]	Tdicdr-Tdicur+1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr-Tdicdr+Tdicur-1.5	Tdicpr-Tdicdr+ Tdicur	Tdicpr-Tdicdr+Tdicur+1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw-Tdicuw-1.5	Tdicdw[6]-Tdicuw[7]	Tdicdw-Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw-Tdicdw+ Tdicuw-1.5	Tdicpw-Tdicdw+ Tdicuw	Tdicpw-Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur-1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr-Tdicdr-1.5	Tdicpr-Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw-1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns

Table 50. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]-Tlbd[10]-Tdicur-1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp-Tlbd-Tdicdr+1.5	—	Tdicpr-Tdicdr-1.5	ns
IP60	Write data setup time	Tds	Tdicdw-1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr-1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw-1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr-1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur-1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw-1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw-1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp-1.5	Tdrp	Tdrp+1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

9 Data read point:

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

10 Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, and an IPU input delay. This value is device specific.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER registers.

4.7.14 Memory Stick Host Controller (MSHC)

Figure 56, Figure 57, and Figure 58 depict the MSHC timings, and Table 51 and Table 52 list the timing parameters.

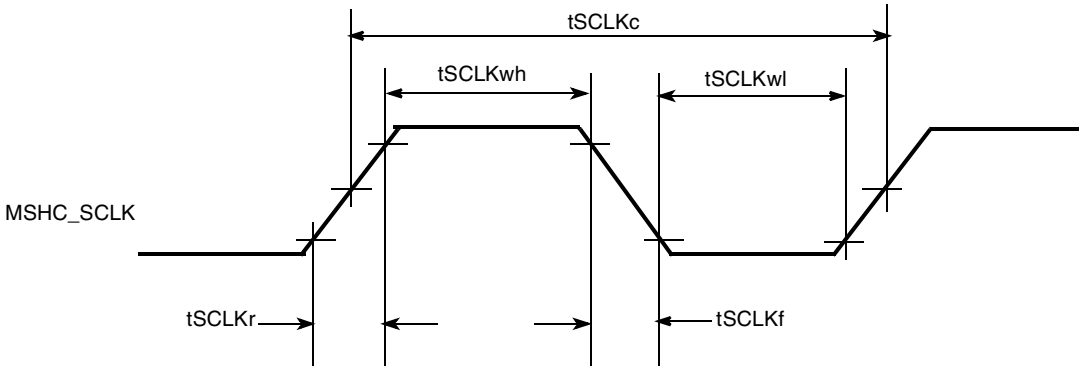


Figure 56. MSHC_CLK Timing Diagram

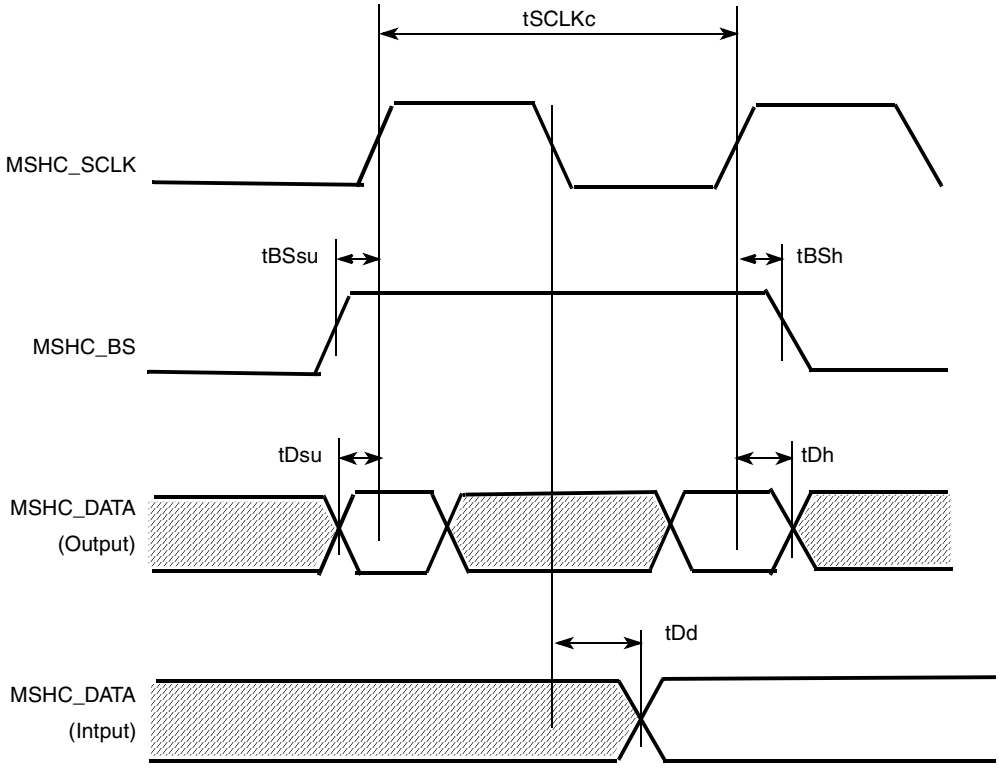


Figure 57. Transfer Operation Timing Diagram (Serial)

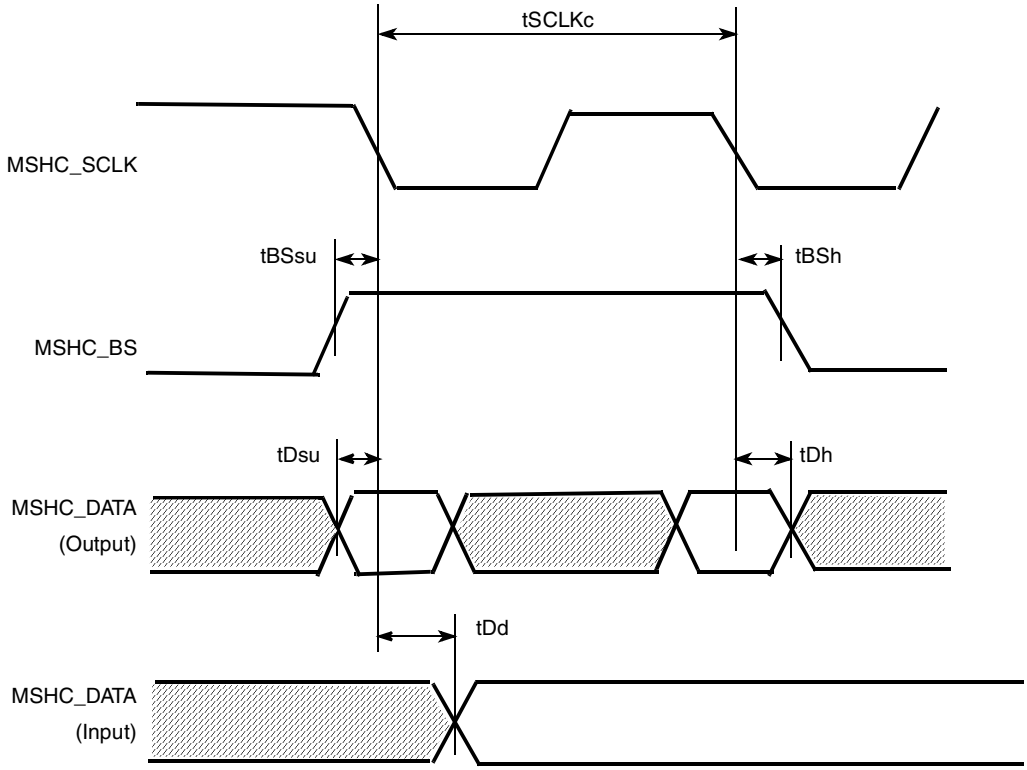


Figure 58. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 51. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 51. Serial Interface Timing Parameters[1] (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 52.

Table 52. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 7, "MCIMX35 Operating Ranges," on page 12.

4.7.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 53. MLB 256/512Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256*fs at 44.0 kHz Typ: 256*fs at 48.0 kHz Typ: 512*fs at 48.0 kHz Max: 512*fs at 48.1 kHz Max: 512*fs PLL unlocked
MLBCLK rise time	t_{mckr}			3	ns	V_{IL} TO V_{IH}

Table 53. MLB 256/512Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLB fall time	t_{mckf}			3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}		81 40		ns	256*Fs 512*Fs
MLBCLK low time	t_{mckl}	31.5 30	37 35.5		ns	256*Fs 256*Fs PLL unlocked
		14.5 14	17 16.5		ns	512*Fs 512*Fs PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5		ns	256*Fs 256*Fs PLL unlocked
		14.5 14	17 16.5		ns	512*Fs 512*Fs PLL unlocked
MLBCLK pulse width variation	t_{mpwv}			2	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1			ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0			ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0		t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	4			ns	Note[3]

1 The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Ground = 0.0V; load capacitance = 40pF; MediaLB speed = 1024Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 54. MLB Device 1024Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	49.152	49.2544 51.200	MHz	Min: 1024*fs at 44.0 kHz Typ: 1024*fs at 48.0 kHz Max: 1024fs*fs at 48.1 kHz Max: 1024*fs PLL unlocked
MLBCLK rise time	t_{mckr}			1	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}			1	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}		20.3		ns	
MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3		ns	PLL unlocked

Table 54. MLB Device 1024Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2		ns	 PLL unlocked
MLBCLK pulse width variation	t_{mpwv}			0.7	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1			ns	
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0			ns	
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0		t_{mckl}	ns	
Bus Hold Time	t_{mdzh}	2			ns	Note[3]

1 The MLB Controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

4.7.16 1-Wire Timing Specifications

Figure 59 depicts the RPP timing, and Table 55 lists the RPP timing parameters.

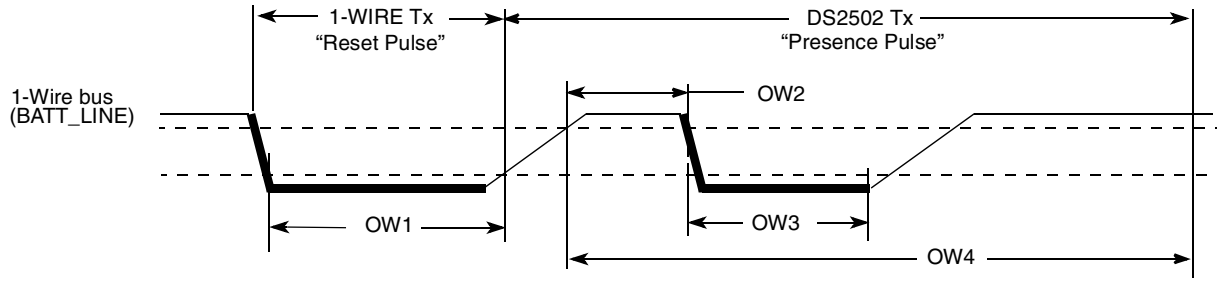


Figure 59. Reset and Presence Pulses (RPP) Timing Diagram

Table 55. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset time low	t_{RSTL}	480	511	—	µs
OW2	Presence detect high	t_{PDH}	15	—	60	µs
OW3	Presence detect low	t_{PDL}	60	—	240	µs
OW4	Reset time high	t_{RSTH}	480	512	—	µs

Figure 60 depicts write 0 sequence timing, and Table 56 lists the timing parameters.

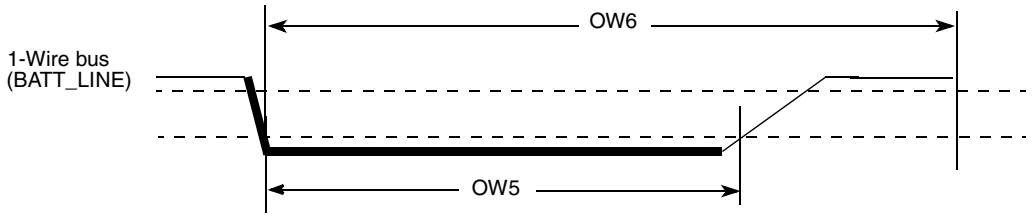


Figure 60. Write 0 Sequence Timing Diagram

Table 56. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 61 shows write 1 sequence timing, Figure 62 depicts the read sequence timing, and Table 57 lists the timing parameters.

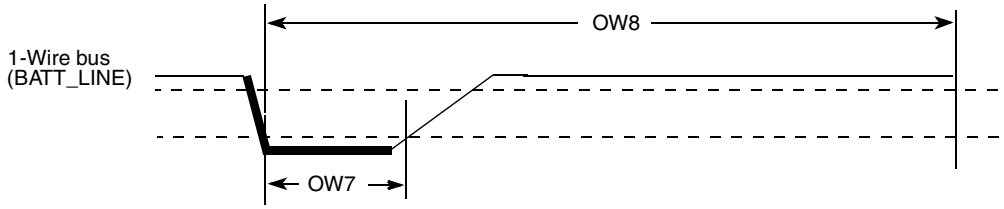


Figure 61. Write 1 Sequence Timing Diagram

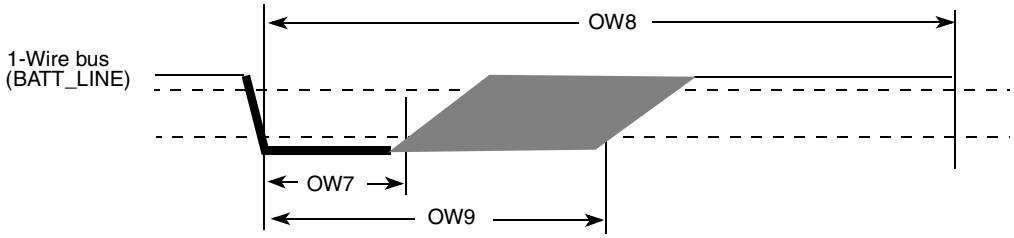


Figure 62. Read Sequence Timing Diagram

Table 57. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1 / read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

4.7.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes. Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.7.17.1 General Timing Requirements

Table 58 and Figure 63 define the AC characteristics of the interface signals on all data transfer modes.

Table 58. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

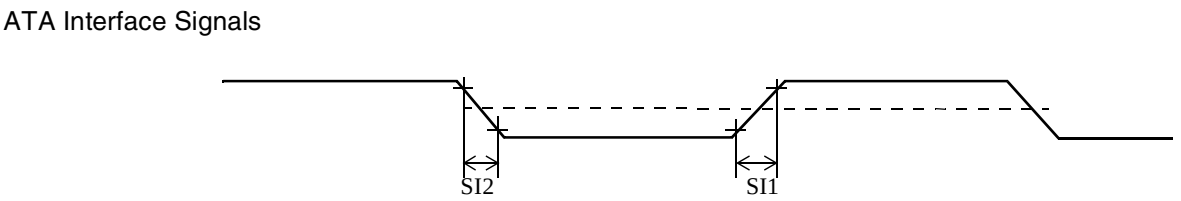


Figure 63. ATA Interface Signals Timing Diagram

4.7.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When ata_buffer_en is negated, the bus drives from device to host. Steering of the signal is such that contention on the host and device tri-state buses is always avoided.

4.7.17.3 Timing Parameters

Table 59 shows the parameters used in the timing equations. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay, and the cable skew.

Table 59. ATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	Peripheral clock frequency
ti_ds	Set-up time **ata_data** to **ata_iordy** edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time **ata_iordy** edge to **ata_data** (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en**	12.0 ns
tsu	Set-up time **ata_data** to bus clock L-to-H	8.5 ns
tsui	Set-up time **ata_iordy** to bus clock H-to-L	8.5 ns
thi	Hold time **ata_iordy** to bus clock H to L	2.5 ns
tskew1	Maximum difference in propagation delay bus clock L-to-H to any of following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en**	7 ns
tskew2	Maximum difference in buffer propagation delay for any of following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en**	Transceiver
tskew3	Maximum difference in buffer propagation delay for any of following signals **ata_iordy, ata_data (read)**	Transceiver
tbuf	Maximum buffer propagation delay	Transceiver
tcable1	Cable propagation delay for **ata_data**	Cable
tcable2	Cable propagation delay for control signals **ata_dior, ata_diow, ata_iordy, ata_dmack**	Cable
tskew4	Maximum difference in cable propagation delay between **ata_iordy** and **ata_data (read)**	Cable
tskew5	Maximum difference in cable propagation delay between (**ata_dior, ata_diow, ata_dmack)** and **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)**	Cable
tskew6	Maximum difference in cable propagation delay without accounting for ground bounce	Cable

[1] Values provided where applicable.

4.7.17.4 PIO Mode Timing

Figure 64 shows timing for PIO read, and Table 60 lists the timing parameters for PIO read.

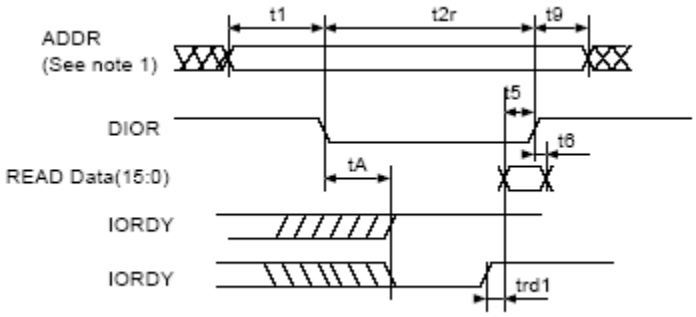


Figure 64. PIO Read Timing Diagram

Table 60. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 64	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 * T - (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min.) = time_2r * T - (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min.) = time_9 * T - (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min.) = (1.5 + time_ax) * T - (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max.) = (–trd) + (tskew3 + tskew4) trd1 (min.) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min.) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 65 shows timing for PIO write, and Table 61 lists the timing parameters for PIO write.

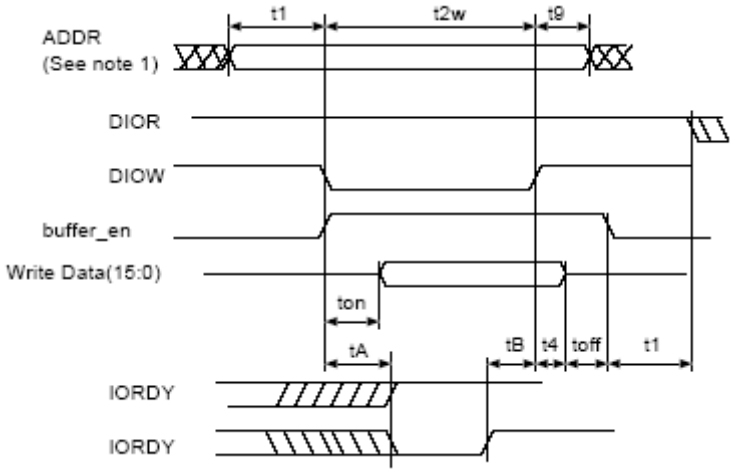


Figure 65. PIO Write Timing Diagram

Table 61. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 65	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min.) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min.) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min.) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min.) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 66 shows timing for MDMA read, Figure 67 shows timing for MDMA write, and Table 62 lists the timing parameters for MDMA read and write.

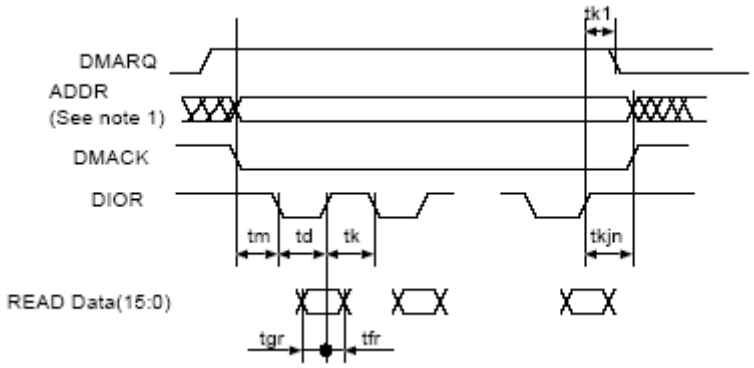


Figure 66. MDMA Read Timing Diagram

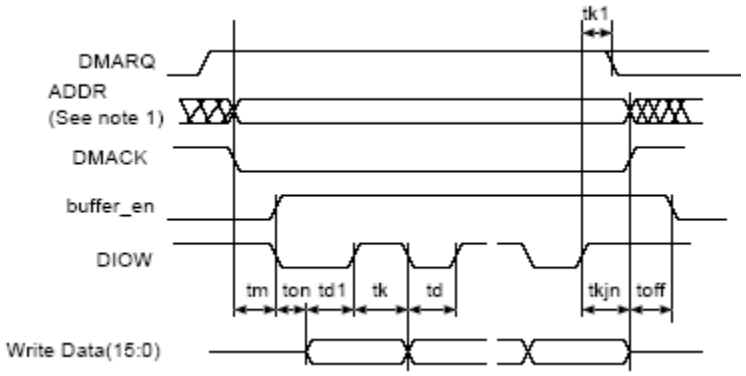


Figure 67. MDMA Write Timing Diagram

Table 62. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 66, Figure 67	Value	Controlling Variable
tm, ti	tm	tm (min.) = ti (min.) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min.) = td (min.) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min.) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min.) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min.-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min.-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min.-drive) = 0	—
tg(write)	—	tg (min.-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min.-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max.) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k

Table 62. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 66, Figure 67	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = (max.(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

4.7.17.5 UDMA-In Timing

Figure 68 shows timing when the UDMA-in transfer starts, Figure 69 shows timing when the UDMA-in host terminates transfer, Figure 70 shows timing when the UDMA-in device terminates transfer, and Table 63 lists the timing parameters for the UDMA-in burst.

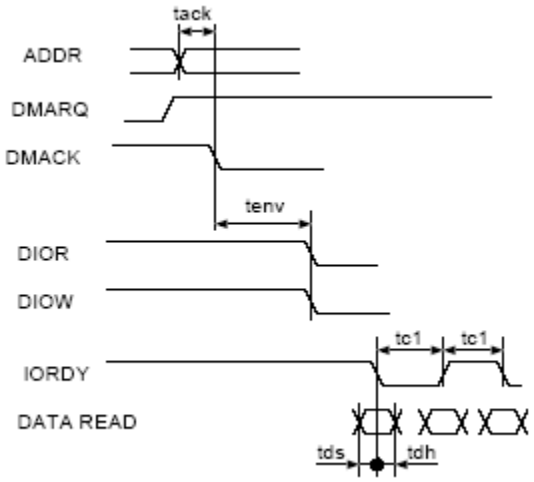


Figure 68. UDMA-In Transfer Starts Timing Diagram

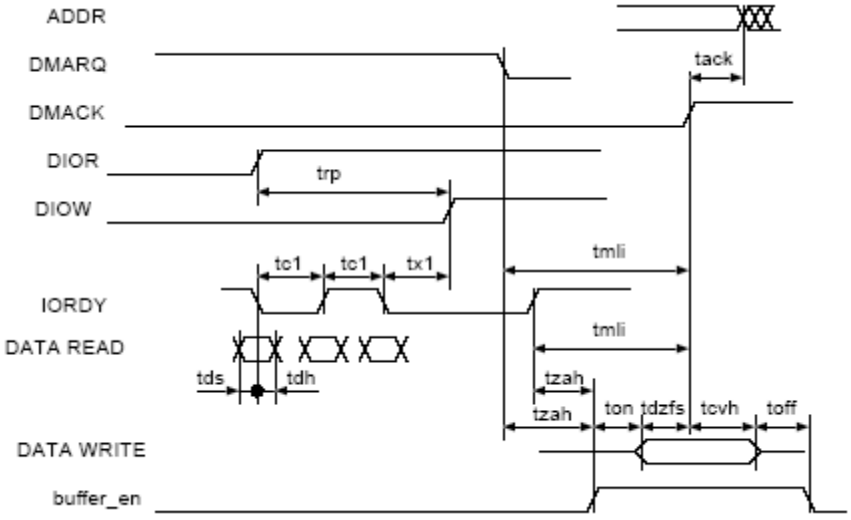


Figure 69. UDMA-In Host Terminates Transfer Timing Diagram

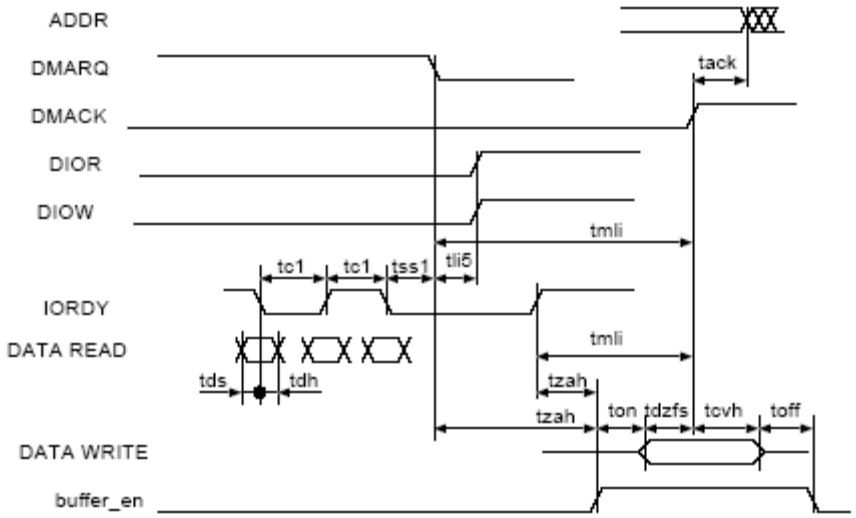


Figure 70. UDMA-In Device Terminates Transfer Timing Diagram

Table 63. UDMA-In Burst Timing Parameters

ATA Parameter	Parameter from Figure 68, Figure 69, Figure 70	Description	Controlling Variable
tack	tack	tack (min.) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env * T) – (tskew1 + tskew2) tenv (max.) = (time_env * T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) –ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min.) = time_rp * T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp * T) – (tco + tsu + 3T + 2 *tbuf + 2*tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min.) = (time_mlix + 0.4) * T	time_mlix
tzah	tzah	tzah (min.) = (time_zah + 0.4) * T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs * T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff big enough to avoid bus contention.

4.7.17.6 UDMA-Out Timing

Figure 71 shows timing when the UDMA-out transfer starts, Figure 72 shows timing when the UDMA-out host terminates transfer, Figure 73 shows timing when the UDMA-out device terminates transfer, and Table 64 lists the timing parameters for the UDMA-out burst.

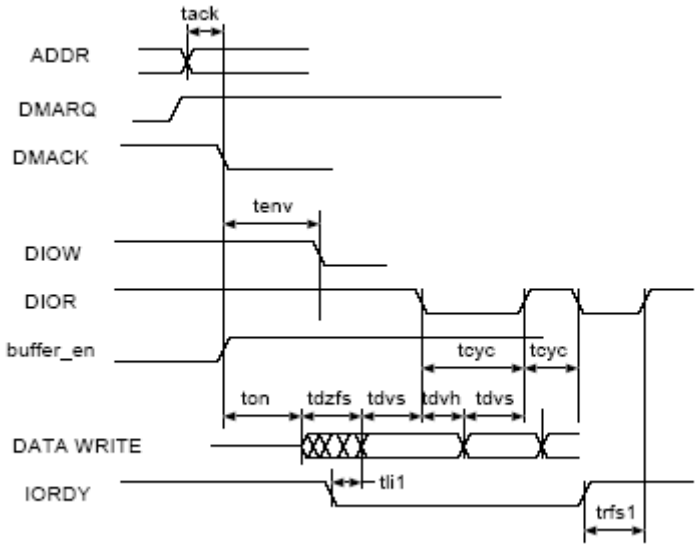


Figure 71. UDMA-Out Transfer Starts Timing Diagram

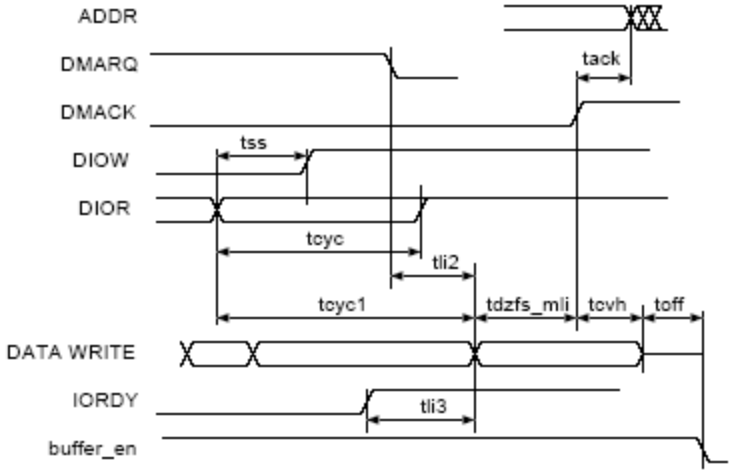


Figure 72. UDMA-Out Host Terminates Transfer Timing Diagram

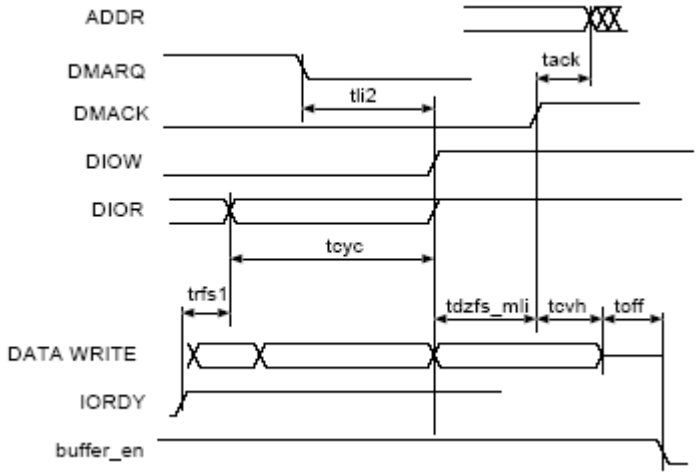


Figure 73. UDMA-Out Device Terminates Transfer Timing Diagram

Table 64. UDMA-Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 71, Figure 72, Figure 73	Value	Controlling Variable
tack	tack	tack (min.) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env * T) – (tskew1 + tskew2) tenv (max.) = (time_env * T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs * T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh * T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc * T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc * 2 * T	time_cyc
trfs1	trfs	trfs = 1.6 * T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs * T – (tskew1)	time_dzfs
tss	tss	tss = time_ss * T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max. (time_dzfs, time_mli) * T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

4.7.18 Parallel Interface (ULPI) Timing

Electrical and timing specifications of the parallel interface are presented in the subsequent sections.

Table 65. Signal Definitions—Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to the clock.
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

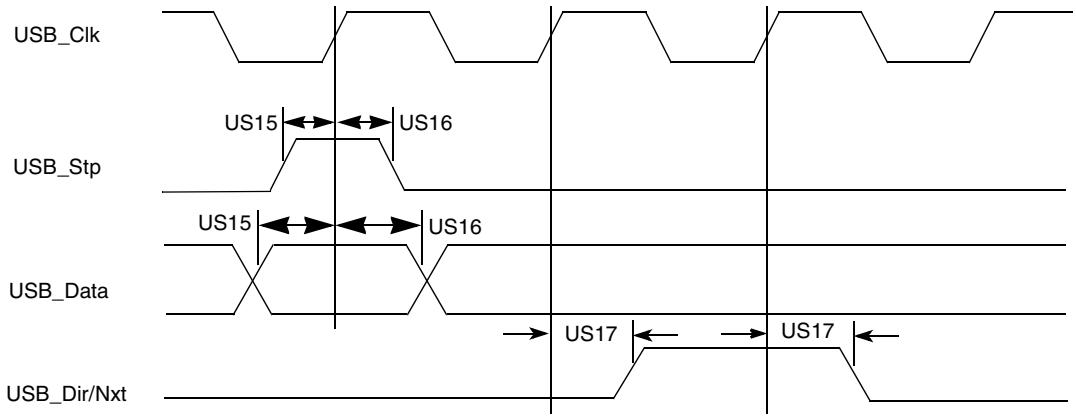


Figure 74. USB Transmit/Receive Waveform in Parallel Mode

Table 66. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Min.	Max.	Unit	Conditions / Reference Signal
US15	USB_TXOE_B	—	6.0	ns	10 pF
US16	USB_DAT_VP	—	0.0	ns	10 pF
US17	USB_SE0_VM	—	9.0	ns	10 pF

4.7.19 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external

pin. The modulated signal of the module is observed at this pin. It can be viewed as a clock signal whose period and duty cycle can be varied with different settings of the PWM. The smallest period is two ipg_clk periods with duty cycle of 50 percent.

4.7.20 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 75 depicts the SJC test clock input timing. Figure 76 depicts the SJC boundary scan timing, Figure 77 depicts the SJC test access port, Figure 78 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 67 lists the SJC timing parameters.

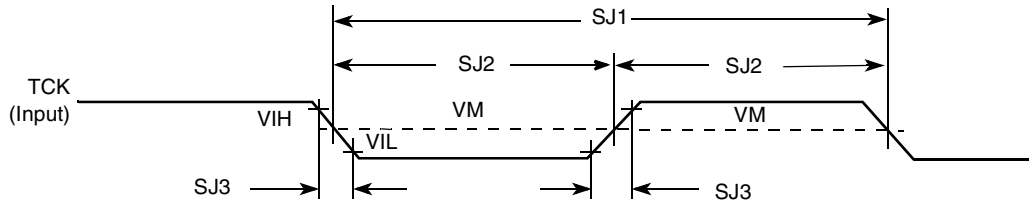


Figure 75. Test Clock Input Timing Diagram

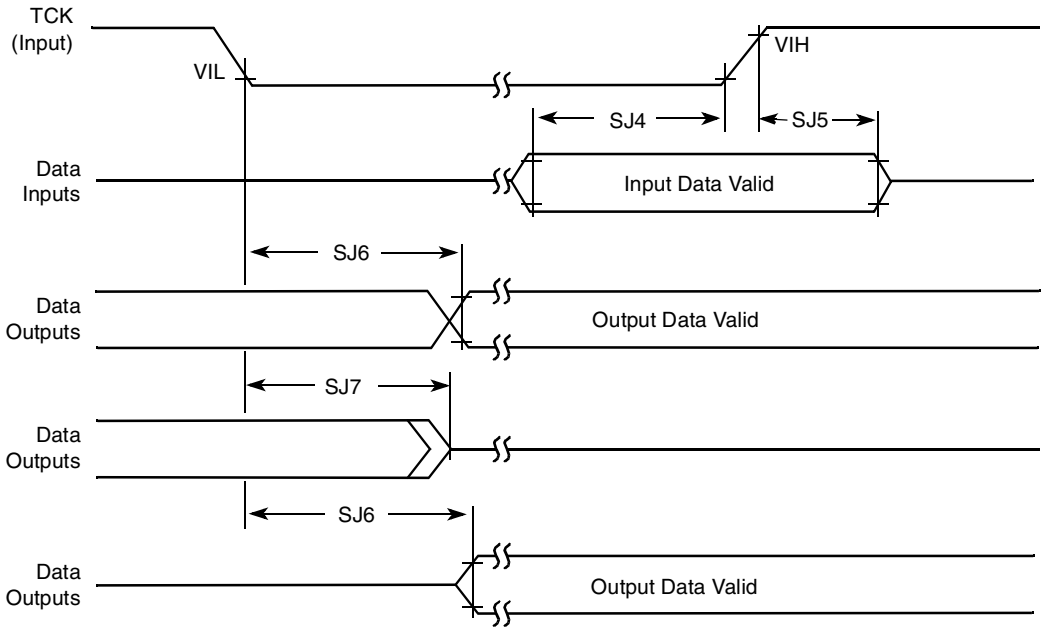


Figure 76. Boundary Scan (JTAG) Timing Diagram

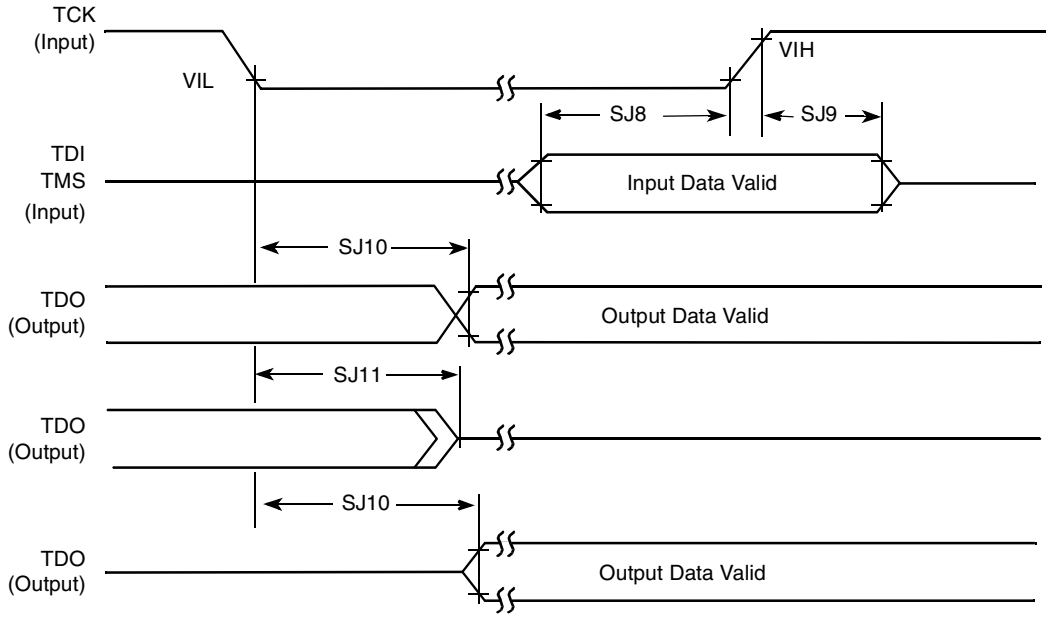


Figure 77. Test Access Port Timing Diagram

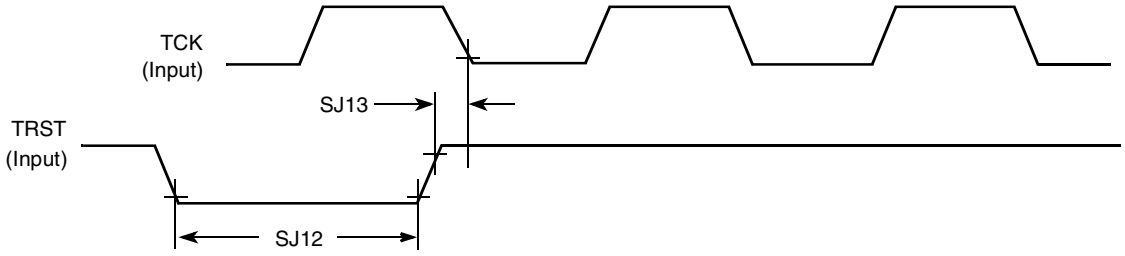


Figure 78. $\overline{\text{TRST}}$ Timing Diagram

Table 67. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

Table 67. SJC Timing Parameters (continued)

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 On cases where SDMA TAP is put in the chain, the max. TCK frequency is limited by max. ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max. frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

2 V_M - mid point voltage

4.7.21 SPDIF Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Figure 79 shows SPDIF timing parameters, including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK). for SPDIF in Tx mode.

Table 68. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Units
		Min.	Max.	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

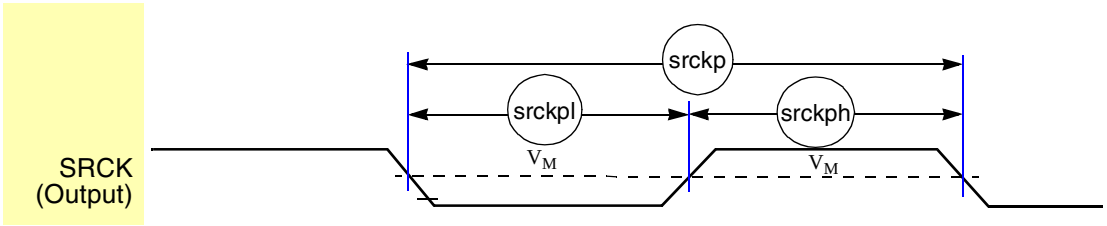
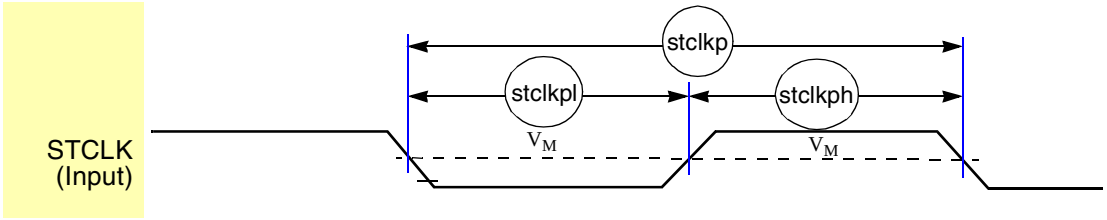


Figure 79. SRCK Timing

Figure 80. STCLK Timing



4.7.22 SSI Electrical Specifications

This section describes electrical characteristics of the SSI.

NOTE

- All of the timing for the SSI is given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timing is on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the transmit and receive sections of the SSI, respectively.
- For internal frame sync operations using the external clock, the FS timing will be the same as that of Tx Data (for example, during AC97 mode of operation).

4.7.22.1 SSI Transmitter Timing with Internal Clock

Figure 81 depicts the SSI transmitter timing with internal clock, and Table 69 lists the timing parameters.

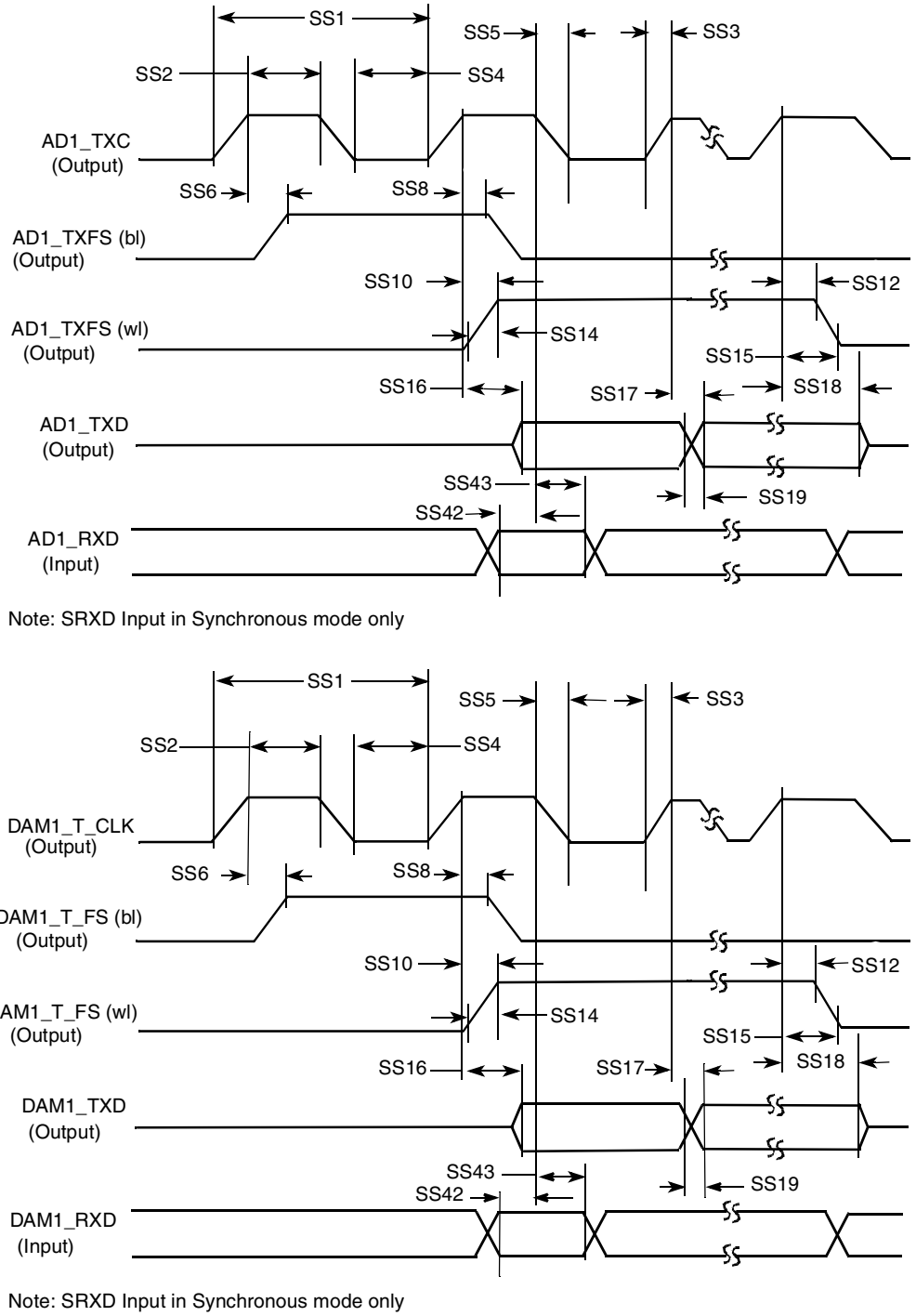


Figure 81. SSI Transmitter with Internal Clock Timing Diagram

Table 69. SSI Transmitter with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6	ns
SS15	(Tx/Rx) Internal FS fall time	—	6	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0	—	ns
SS52	Loading	—	25	pF

4.7.22.2 SSI Receiver Timing with Internal Clock

Figure 82 depicts the SSI receiver timing with internal clock. Table 70 lists the timing parameters shown in Figure 82.

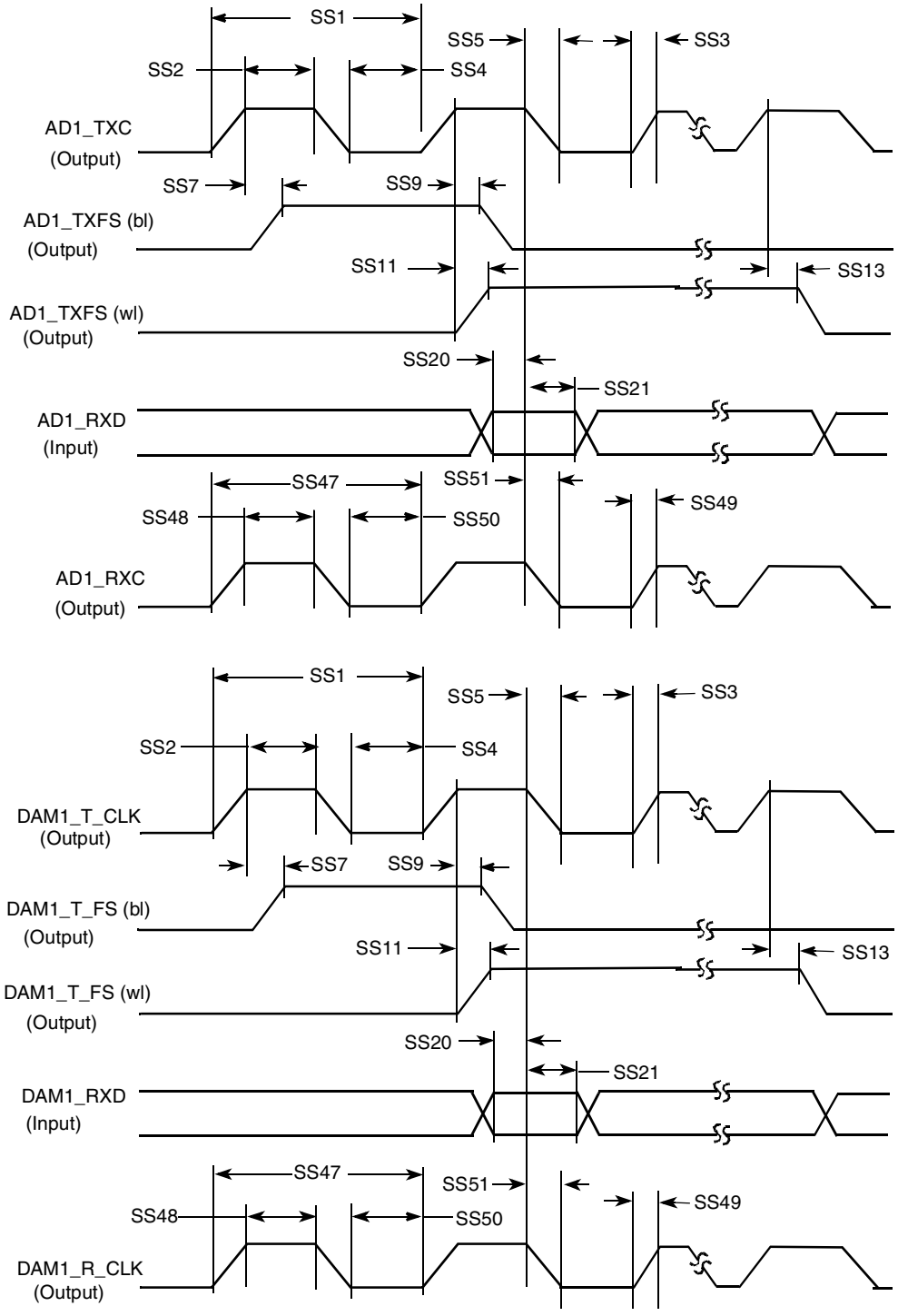


Figure 82. SSI Receiver with Internal Clock Timing Diagram

Table 70. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

4.7.22.3 SSI Transmitter Timing with External Clock

Figure 83 depicts the SSI transmitter timing with external clock, and Table 71 lists the timing parameters.

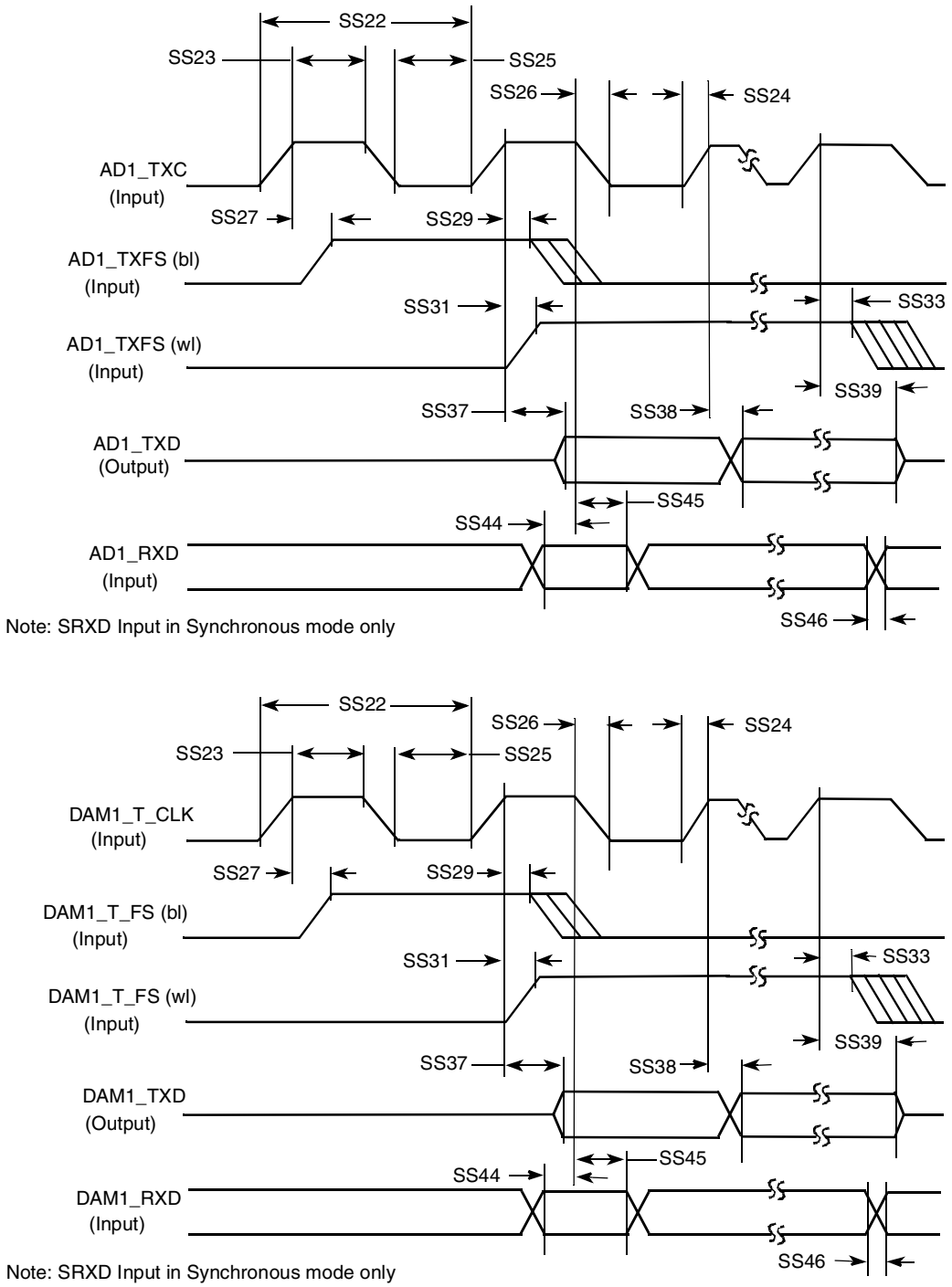


Figure 83. SSI Transmitter with External Clock Timing Diagram

Table 71. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	—10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

4.7.22.4 SSI Receiver Timing with External Clock

Figure 84 depicts the SSI receiver timing with external clock, and Table 72 lists the timing parameters.

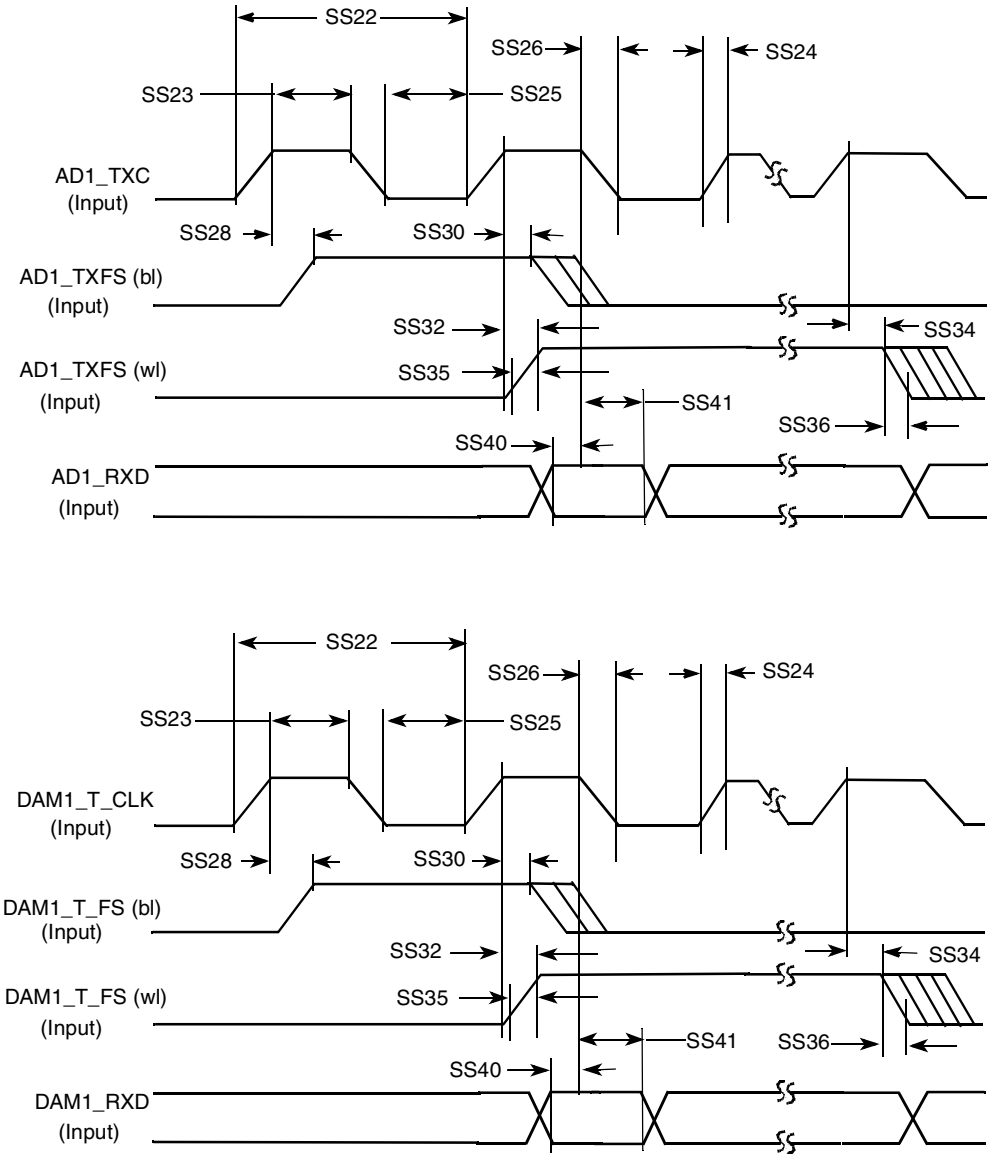


Figure 84. SSI Receiver with External Clock Timing Diagram

Table 72. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns

Table 72. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min.	Max.	Unit
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.7.23 UART Electrical

This section describes the electrical information of the UART module.

4.7.23.1 UART RS-232 Serial Mode Timing

4.7.23.1.11 UART Transmitter

Figure 85 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 73 lists the UART RS-232 serial mode transmit timing characteristics.

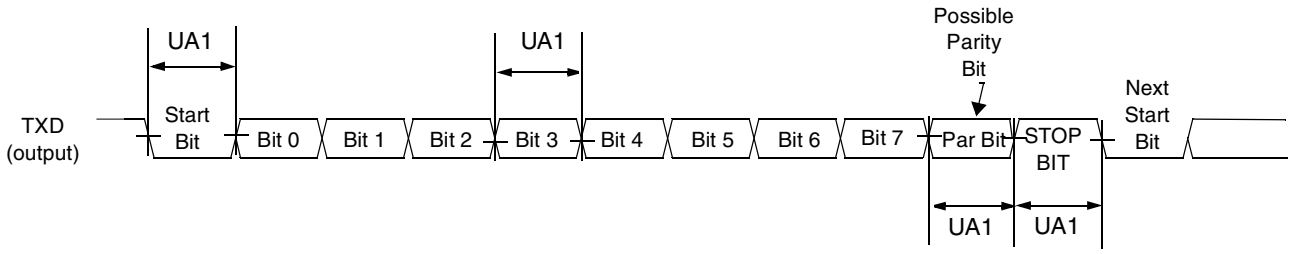


Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 73. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate}$ + T_{ref_clk}	-

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.23.1.12 UART Receiver

Figure 86 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 74 lists serial mode receive timing characteristics.

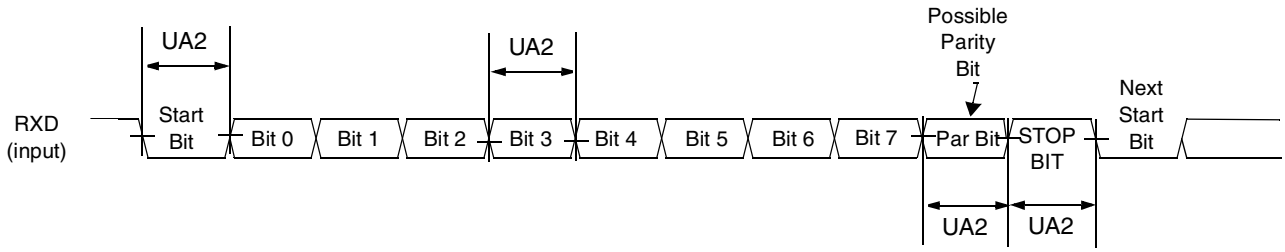


Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 74. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate}$ + $1/(16*F_{baud\_rate})$	-

1 Note: The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.23.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.23.2.13 UART IrDA Mode Transmitter

Figure 87 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 75 lists the transmit timing characteristics.

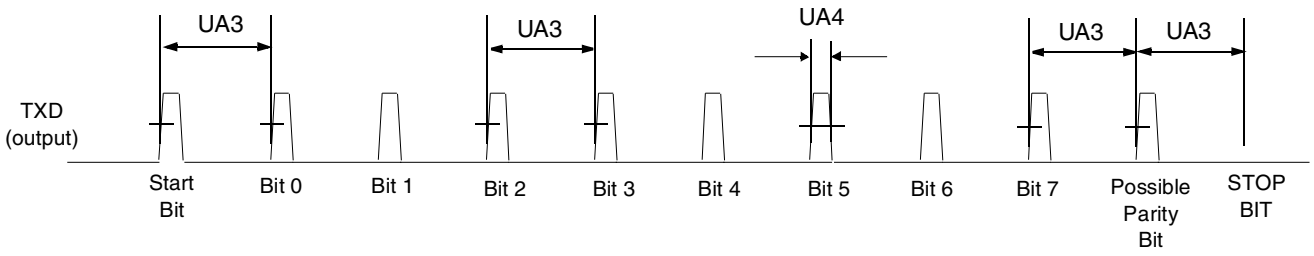


Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 75. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	-
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	-

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.23.2.14 UART IrDA Mode Receiver

Figure 88 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 76 lists the receive timing characteristics.

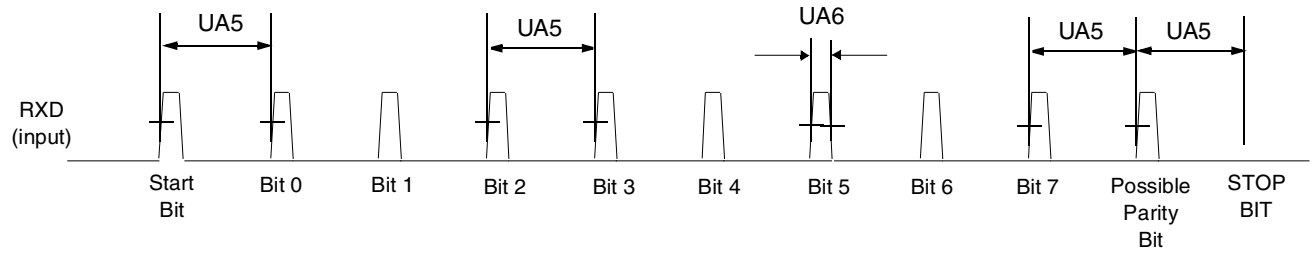


Figure 88. UART IrDA Mode Receive Timing Diagram

Table 76. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate}$ + $1/(16*F_{baud\_rate})$	-
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 us	$(5/16)*(1/F_{baud\_rate})$	-

1 The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.24 USB Electrical Specifications

In order to support four different serial interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

4.7.24.1 DAT_SE0 Bidirectional Mode

Table 77. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

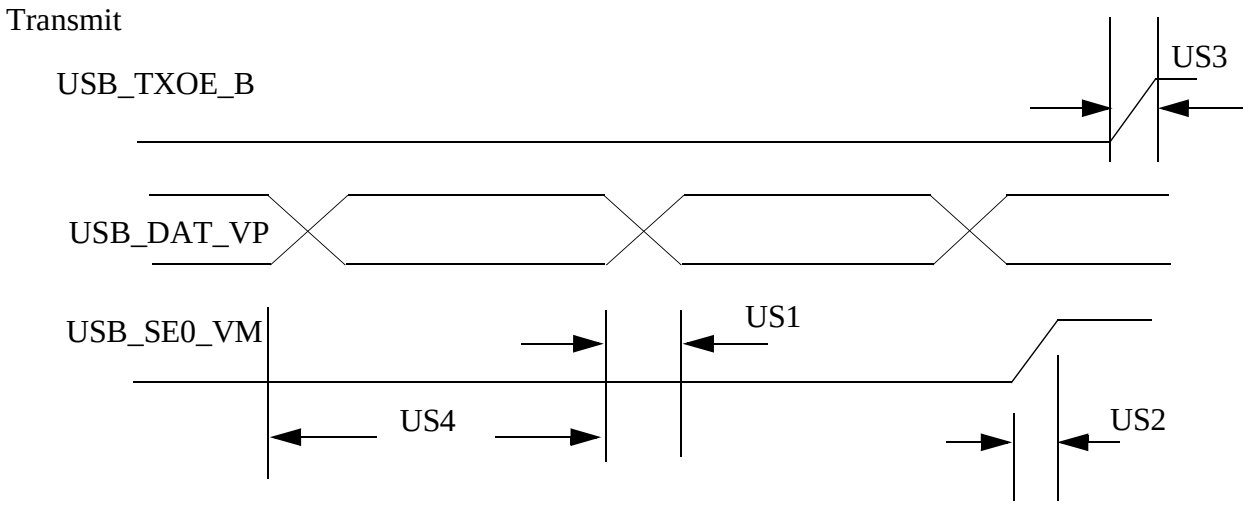


Figure 89. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

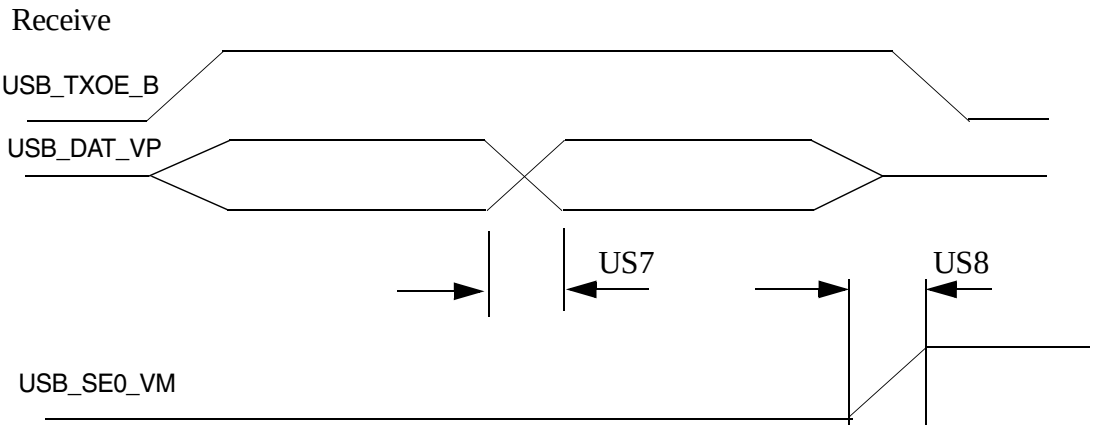


Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 78. Signal Definitions—DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions / Reference Signal
US1	Tx Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	Rx Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.24.2 DAT_SE0 Unidirectional Mode

Table 79. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

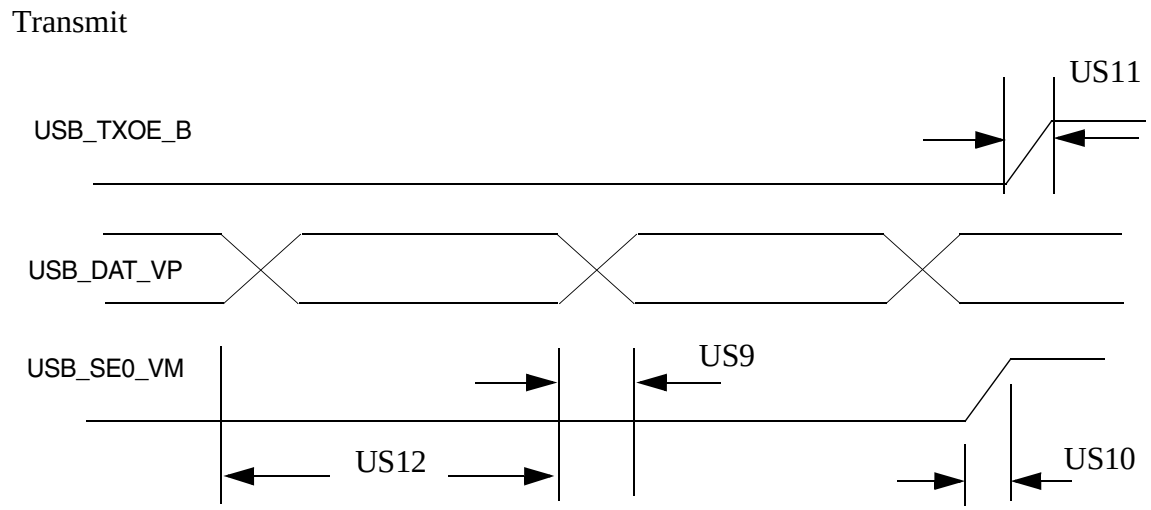


Figure 91. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

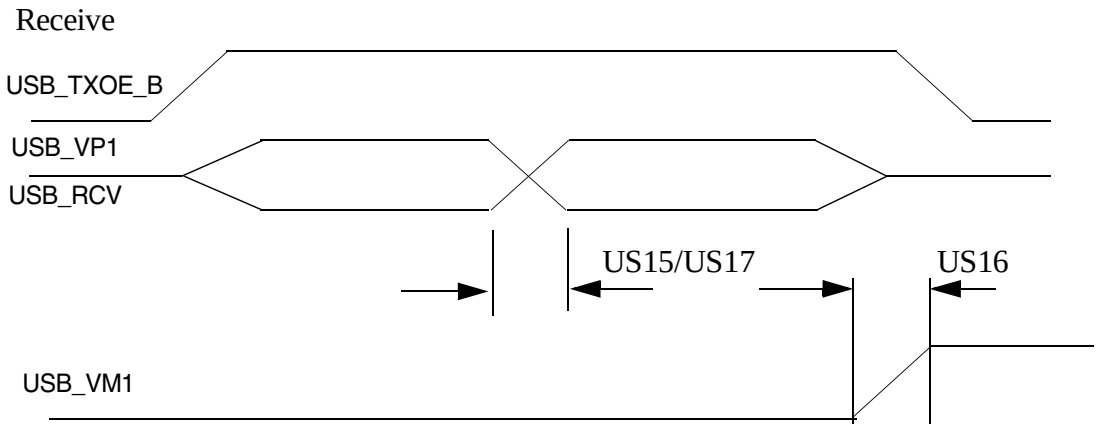


Figure 92. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 80. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min.	Max.	Unit	Condition / Reference Signal
US9	Tx Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	Tx Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	Tx Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	Tx Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	Rx Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	Rx Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US17	Rx Rise/Fall Time	USB_RCV	In	—	3.0	ns	35 pF

4.7.24.3 VP_VM Bidirectional Mode

Table 81. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	Tx VP data when USB_TXOE_B is low Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	Tx VM data when USB_TXOE_B low Rx VM data when USB_TXOE_B high
USB_RCV	In	Differential Rx data

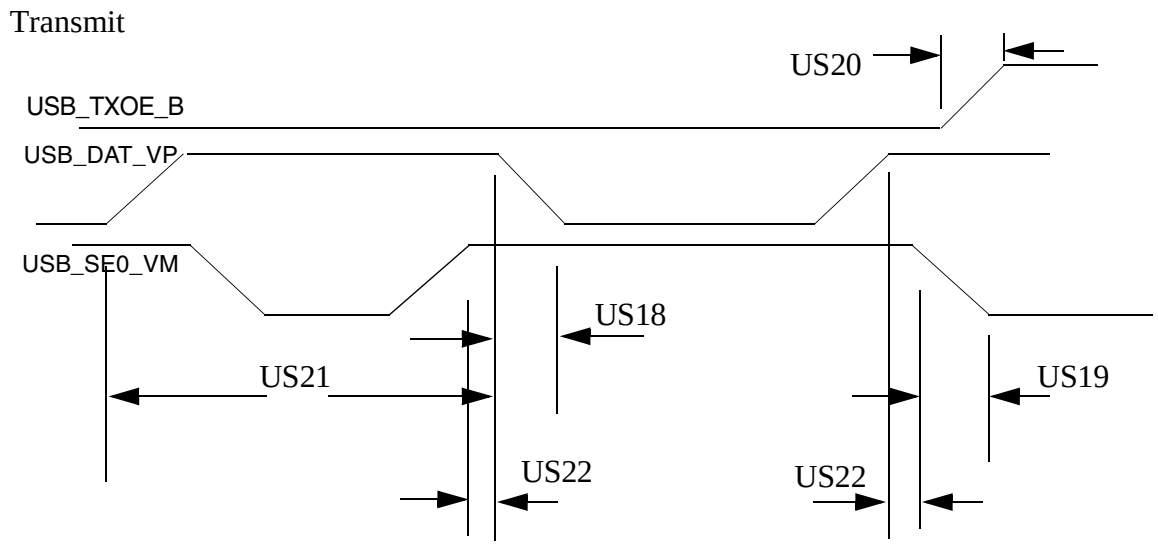


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

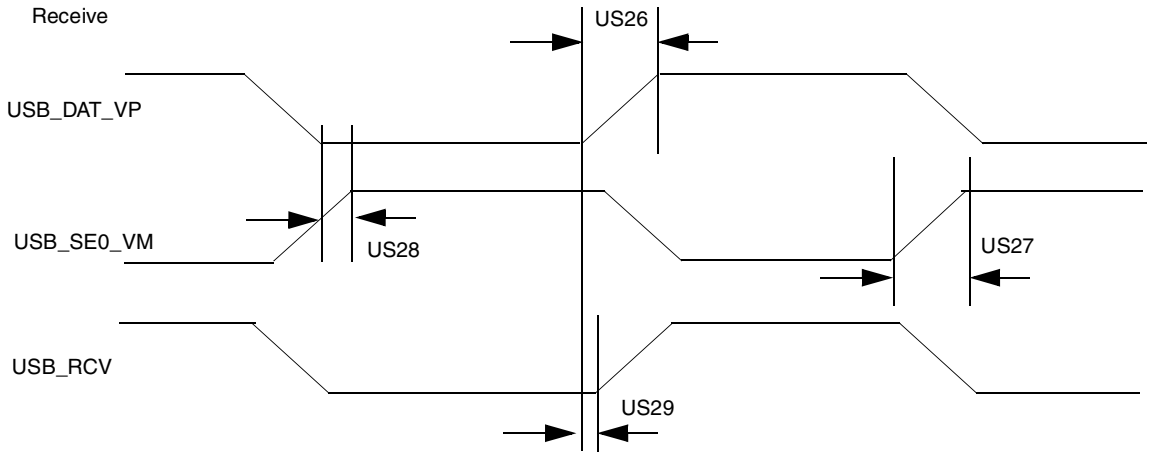


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 82. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition / Reference Signal
US18	Tx Rise/Fall Time	USB_DAT_VP	Out	-	5.0	ns	50 pF
US19	Tx Rise/Fall Time	USB_SE0_VM	Out	-	5.0	ns	50 pF
US20	Tx Rise/Fall Time	USB_TXOE_B	Out	-	5.0	ns	50 pF
US21	Tx Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	-
US22	Tx Overlap	USB_SE0_VM	Out	-3.0	+3.0	ns	USB_DAT_VP
US26	Rx Rise/Fall Time	USB_DAT_VP	In	-	3.0	ns	35 pF
US27	Rx Rise/Fall Time	USB_SE0_VM	In	-	3.0	ns	35 pF
US28	Rx Skew	USB_DAT_VP	In	-4.0	+4.0	ns	USB_SE0_VM
US29	Rx Skew	USB_RCV	In	-6.0	+2.0	ns	USB_DAT_VP

4.7.24.4 VP_VM Unidirectional Mode

Table 83. Signal Definitions—VP_VM Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx VP data when USB_TXOE_B is low
USB_SE0_VM	Out	Tx VM data when USB_TXOE_B is low
USB_VP1	In	Rx VP data when USB_TXOE_B is high
USB_VM1	In	Rx VM data when USB_TXOE_B is high
USB_RCV	In	Differential Rx data

Transmit

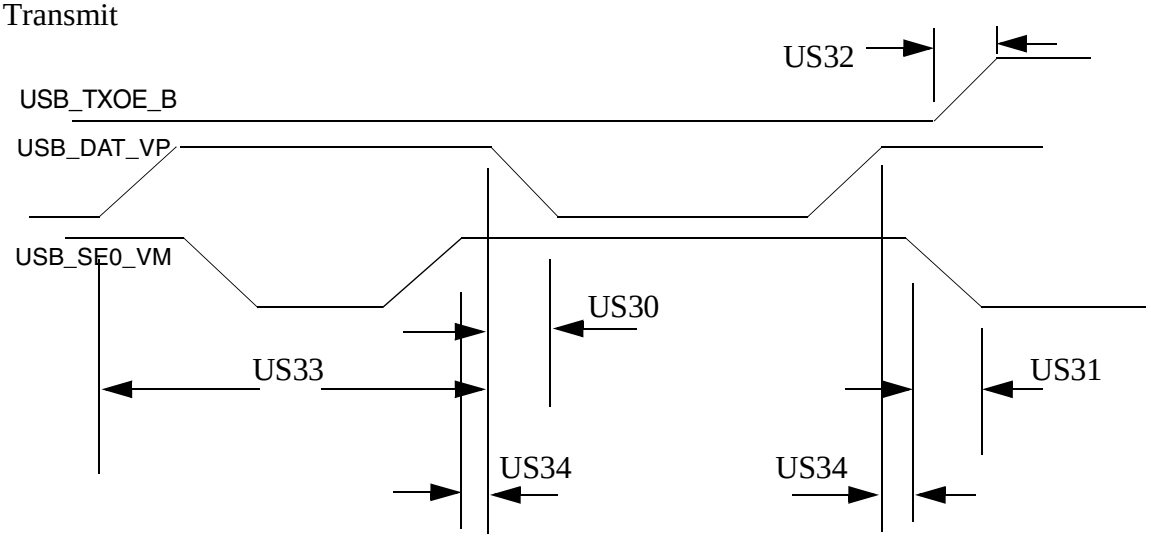


Figure 95. USB Transmit Waveform in VP_VM Unidirectional Mode

Receive

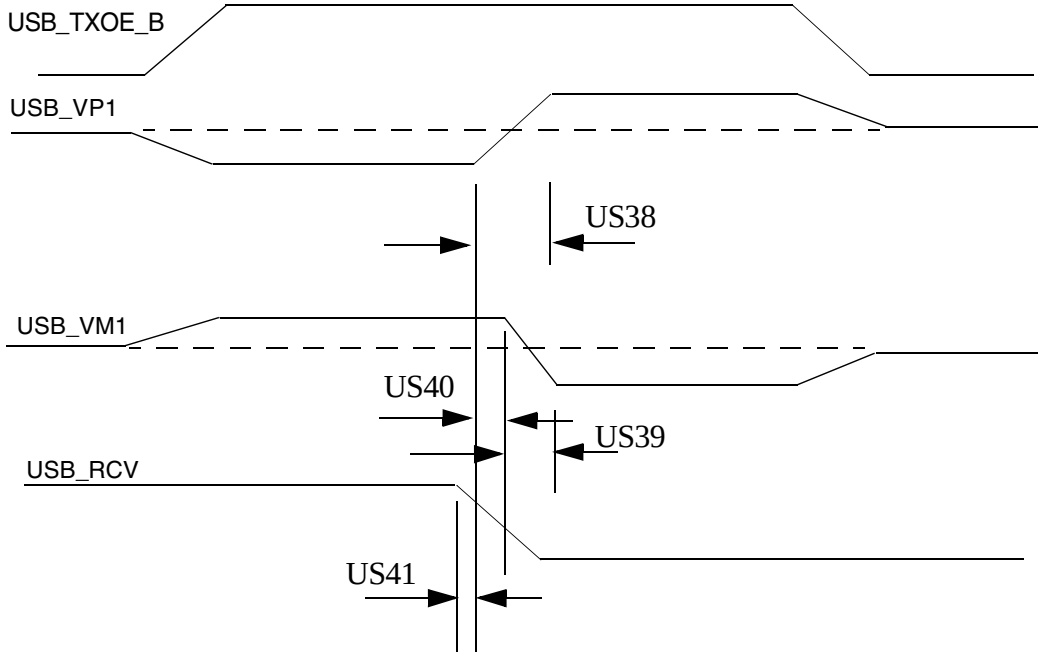


Figure 96. USB Receive Waveform in VP_VM Unidirectional Mode

Table 84. USB Timing Specification in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions / Reference Signal
US30	Tx Rise/Fall Time	USB_DAT_VP	Out	-	5.0	ns	50 pF
US31	Tx Rise/Fall Time	USB_SE0_VM	Out	-	5.0	ns	50 pF
US32	Tx Rise/Fall Time	USB_TXOE_B	Out	-	5.0	ns	50 pF
US33	Tx Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	-
US34	Tx Overlap	USB_SE0_VM	Out	-3.0	+3.0	ns	USB_DAT_VP
US38	Rx Rise/Fall Time	USB_VP1	In	-	3.0	ns	35 pF
US39	Rx Rise/Fall Time	USB_VM1	In	-	3.0	ns	35 pF
US40	Rx Skew	USB_VP1	In	-4.0	+4.0	ns	USB_VM1
US41	Rx Skew	USB_RCV	In	-6.0	+2.0	ns	USB_VP1

5 Package Information and Pinout

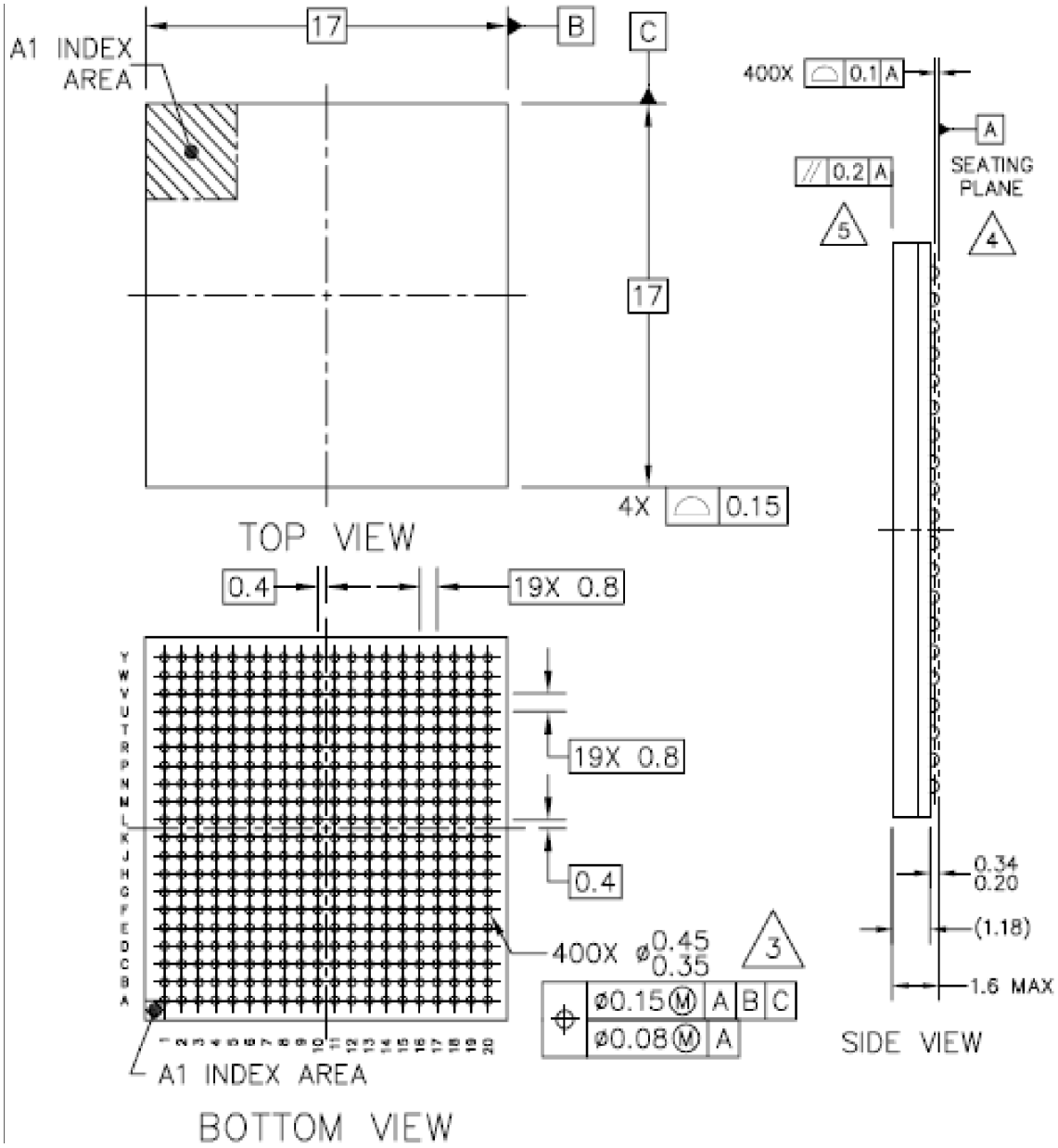
This section includes the following:

- Pin/contact assignment information
- Mechanical package drawing

5.1 MAPBGA Production Package 1568-01, 17 x 17 mm, 0.8 Pitch

See Figure 97 for the package drawing and dimensions of the production package.

5.2 Production Package Outline Drawing



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 97. Production Package: Mechanical Drawing

5.2.1 MAPBGA Signal Assignments

Table 85 lists MAPBGA signals alphabetized by signal name. Table 86 shows the signal assignment on the MCIMX35 ball map.

Table 85. Signal Ball Map Locations

Signal ID	Ball Location
A0	A5
A1	D7
A10	F15
A11	D5
A12	F6
A13	B3
A14	D14
A15	D15
A16	D13
A17	D12
A18	E11
A19	D11
A2	E7
A20	D10
A21	E10
A22	D9
A23	E9
A24	D8
A25	E8
A3	C6
A4	D6
A5	B5
A6	C5
A7	A4
A8	B4
A9	A3
ATA_BUFF_EN	T5
ATA_CS0	V7
ATA_CS1	T7
ATA_DA0	R4
ATA_DA1	V1
ATA_DA2	R5
ATA_DATA0	Y5
ATA_DATA1	W5
ATA_DATA10	V3
ATA_DATA11	Y2
ATA_DATA12	U3
ATA_DATA13	W2
ATA_DATA14	W1
ATA_DATA15	T4
ATA_DATA2	V5

Signal ID	Ball Location
ATA_DATA7	Y3
ATA_DATA8	U4
ATA_DATA9	W3
ATA_DIOR	Y6
ATA_DIOW	W6
ATA_DMACK	V6
ATA_DMARQ	T3
ATA_INTRQ	V2
ATA_IORDY	U6
ATA_RESET_B	T6
BCLK	E14
BOOT_MODE0	W10
BOOT_MODE1	U9
CAPTURE	V12
CAS	E16
CLK_MODE0	Y10
CLK_MODE1	T10
CLKO	V10
COMPARE	T12
CONTRAST	L16
CS0	F17
CS1	E19
CS2	B20
CS3	C19
CS4	E18
CS5	F19
CSI_D10	V16
CSI_D11	T15
CSI_D12	W16
CSI_D13	V15
CSI_D14	U14
CSI_D15	Y16
CSI_D8	U15
CSI_D9	W17
CSI_HSYNC	V14
CSI_MCLK	W15
CSI_PIXCLK	Y15
CSI_VSYNC	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8

Table 85. Signal Ball Map Locations (continued)

Signal ID	Ball Location
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS	L17
D3_DRDY	L20
D3_FPSHIFT	L15
D3_HSYNC	L18
D3_REV	M17
D3_SPL	M18
D3_VSYNC	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
DQM1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3

Signal ID	Ball Location
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0	F20
LD1	G18
LD10	H20
LD11	J18
LD12	J16
LD13	J19
LD14	J17
LD15	J20
LD16	K14
LD17	K19
LD18	K18
LD19	K20
LD2	G17
LD20	K16
LD21	K17
LD22	K15
LD23	L19
LD3	G16
LD4	G19
LD5	H16

Table 85. Signal Ball Map Locations (continued)

Signal ID	Ball Location
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NGND_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11
NVCC_EMI1	G7
NVCC_EMI1	G8
NVCC_EMI1	G9
NVCC_EMI1	H9

Signal ID	Ball Location
LD6	H18
LD7	G20
LD8	H17
LD9	H19
NVCC_EMI2	G12
NVCC_EMI2	F13
NVCC_EMI2	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
RAS	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20
RXD1	U2
RXD2	H3
SCK4	L4
SCK5	L5

Table 85. Signal Ball Map Locations (continued)

Signal ID	Ball Location
NVCC_EMI1	F10
NVCC_EMI1	G10
NVCC_EMI1	F11
NVCC_EMI1	G11
SD1_CLK	V18
SD1_CMD	Y19
SD1_DATA0	R14
SD1_DATA1	U16
SD1_DATA2	W18
SD1_DATA3	V17
SD10	A15
SD11	B15
SD12	C13
SD13	B14
SD14	A14
SD15	B13
SD16	C12
SD17	C11
SD18	A12
SD19	B12
SD2	B18
SD2_CLK	W14
SD2_CMD	U13
SD2_DATA0	V13
SD2_DATA1	T13
SD2_DATA2	Y14
SD2_DATA3	U12
SD20	B11
SD21	A11
SD22	C10
SD23	B10
SD24	A9
SD25	C9
SD26	B9
SD27	A8
SD28	B8
SD29	C8
SD3	C16
SD30	A7
SD31	B7
SD4	A18
SD5	C15
SD6	A17
SD7	B16
SD8	C14
SD9	A16

Signal ID	Ball Location
SCKR	K3
SCKT	J4
SD0	C17
SD1	A19
SDCLK	E12
SDCLK_B	E13
SDQS0	B17
SDQS1	A13
SDQS2	A10
SDQS3	C7
SDWE	G15
SJC_MOD	U17
SRXD4	L1
SRXD5	K4
STXD4	M2
STXD5	K1
STXFS4	L2
STXFS5	J6
TCK	R17
TDI	P15
TDO	R15
TEST_MODE	Y7
TMS	R16
TRSTB	T16
TTM_PAD	M16
TX0	G4
TX1	H1
TX2_RX3	H5
TX3_RX2	J2
TX4_RX1	H4
TX5_RX0	J3
TXD1	R6
TXD2	H2
USBOTG_OC	U7
USBOTG_PWR	W7
USBPHY1_DM	N19
USBPHY1_DP	P19
USBPHY1_RREF	R19
USBPHY1_UID	N18
USBPHY1_UPLLGND	N14
USBPHY1_UPLLVDD	N15
USBPHY1_UPLLVDD	P17
USBPHY1_VBUS	P18
USBPHY1_VDDA_BIAS	R20
USBPHY1_VSSA_BIAS	R18
USBPHY2_DM	Y17

Table 85. Signal Ball Map Locations (continued)

Signal ID	Ball Location
SDBA0	A6
SDBA1	B6
SDCKE0	D18
SDCKE1	E17
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
USBPHY2_DP	Y18
VDD	M6
VDD	F7
VDD	J7
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
VSS	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

Table 86. Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	D0	A9	A7	A0	SDBA 0	SD30	SD27	SD24	SDQ S2	SD21	SD18	SDQ S1	SD14	SD10	SD9	SD6	SD4	SD1	VSS	A
B	D5	D2	A13	A8	A5	SDBA 1	SD31	SD28	SD26	SD23	SD20	SD19	SD15	SD13	SD11	SD7	SDQ S0	SD2	DQM 0	CS2	B
C	D8	D7	D4	MA10	A6	A3	SDQ S3	SD29	SD25	SD22	SD17	SD16	SD12	SD8	SD5	SD3	SD0	DQM 3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A20	A19	A17	A16	A14	A15	DQM 2	DQM 1	SDCK E0	ECB	LBA	D
E	NFCL E	D15	D12	D9	D3	D11	A2	A25	A23	A21	A18	SDCL K	SDCL K_B	BCLK	RAS	CAS	SDCK E1	CS4	CS1	OE	E
F	NFRE _B	NFAL E	NFRB	NFW P_B	D13	A12	VDD	VDD	VDD	NVC C_EM I1	NVC C_EM I1	VDD	NVC C_EM I2	NVC C_EM I2	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFW E_B	NF_C E0	TX0	CTS2	NVC C_NF C	NVC C_EM I1	NVC C_EM I1	NVC C_EM I1	NVC C_EM I1	NVC C_EM I1	NVC C_EM I2	VDD	NVC C_EM I3	SDW E	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_ RX1	TX2_ RX3	NVC C_NF C	NVC C_NF C	NGN D_EM I1	NVC C_EM I1	NGN D_EM I1	VSS	VSS	VSS	NVC C_LC DC	VDD	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_ RX2	TX5_ RX0	SCKT	HCKT	STXF S5	VDD	VSS	VSS	NGN D_EM I1	NGN D_EM I2	NGN D_EM I3	VSS	NVC C_LC DC	VDD	LD12	LD14	LD11	LD13	LD15	J
K	STXD 5	HCK R	SCKR	SRXD 5	FSR	NVC C_MI SC	NVC C_MI SC	NGN D_MI SC	NGN D_NF C	VSS	NGN D_LC DC	NGN D_EM I3	VSS	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD 4	STXF S4	I2C2_ CLK	SCK4	SCK5	FEC_ TDAT A3	VDD	NVC C_MI SC	VSS	NGN D_AT A	NGN D_CR M	NGN D_LC DC	VSS	NVC C_LC DC	D3_F PSHI FT	CON TRAS T	D3_C LS	D3_H SYNC	LD23	D3_D RDY	L
M	I2C2_ DAT	STXD 4	FEC_ RDAT A2	FEC_ TDAT A1	FEC_ TDAT A2	VDD	NGN D_MI SC	VSS	NGN D_AT A	NGN D_ML B	FUSE _VSS	PGN D	NGN D_JT AG	NVC C_LC DC	PHY1 _VDD A	TTM_ PAD	D3_R EV	D3_S PL	D3_V SYNC	I2C1_ CLK	M
N	FEC_ RDAT A3	FEC_ RDAT A1	FEC_ RX_E RR	FEC_ TX_E RR	FEC_ CRS	NVC C_AT A	VDD	VSS	VSS	NGN D_CS I	MGN D	NGN D_SD IO	PVDD	USBP HY1_ UPLL GND	USBP HY1_ UPLL VDD	PHY1 _VSS A	I2C1_ DAT	USBP HY1_ UID	USBP HY1_ DM	PHY1 _VDD A	N
P	FEC_ MDIO	FEC_ RDAT A0	FEC_ COL	FEC_ TX_C LK	FEC_ TDAT A0	NVC C_AT A	NVC C_AT A	NVC C_AT A	NGN D_AT A	VSS	MVD D	PHY2 _VSS	FUSE _VDD	NVC C_SD IO	TDI	NVC C_JT AG	USBP HY1_ UPLL VDD	USBP HY1_ VBUS	USBP HY1_ DP	PHY1 _VSS A	P
R	FEC_ MDC	FEC_ RX_C LK	CTS1	ATA_ DA0	ATA_ DA2	TXD1	VDD	VDD	NVC C_CR M	NVC C_ML B	NVC C_CS I	VDD	PHY2 _VDD	SD1_ DATA 0	TDO	TMS	TCK	USBP HY1_ VSSA _BIA S	USBP HY1_ RREF	USBP HY1_ VDDA _BIA S	R
T	FEC_ TX_E N	FEC_ RX_D V	ATA_ DMA RQ	ATA_ DATA 15	ATA_ BUFF _EN	ATA_ RESE T_B	ATA_ CS1	CSPI 1_SPI _RDY	VSTB Y	CLK_ MOD E1	GPIO 1_0	COM PARE	SD2_ DATA 1	CSI_ VSYN C	CSI_ D11	TRST B	VSS	OSC2 4M_V SS	OSC2 4M_V DD	EXTA L24M	T
U	RTS1	RXD1	ATA_ DATA 12	ATA_ DATA 8	ATA_ DATA 3	ATA_I ORDY	USB OTG_ OC	CSPI 1_SS 1	BOOT _MO DE1	RESE T_IN_ B	GPIO 2_0	SD2_ DATA 3	SD2_ CMD	CSI_ D14	CSI_ D8	SD1_ DATA 1	SJC_ MOD	RTCK	OSC_ AUDI O_VS S	XTAL 24M	U
V	ATA_ DA1	ATA_I NTR Q	ATA_ DATA 10	ATA_ DATA 6	ATA_ DATA 2	ATA_ DMA CK	ATA_ CS0	EXT_ ARM CLK	CSPI 1_MI SO	CLKO	GPIO 3_0	CAPT URE	SD2_ DATA 0	CSI_ HSYN C	CSI_ D13	CSI_ D10	SD1_ DATA 3	SD1_ CLK	XTAL _AUD IO	OSC_ AUDI O_VD D	V
W	ATA_ DATA 14	ATA_ DATA 13	ATA_ DATA 9	ATA_ DATA 5	ATA_ DATA 1	ATA_ DIOW	USB OTG_ PWR	CSPI 1_SC LK	CSPI 1_MO SI	BOOT _MO DE0	POR_ B	MLB_ SIG	MLB_ CLK	SD2_ CLK	CSI_ MCLK	CSI_ D12	CSI_ D9	SD1_ DATA 2	DE_B	EXTA L_AU DIO	W
Y	VSS	ATA_ DATA 11	ATA_ DATA 7	ATA_ DATA 4	ATA_ DATA 0	ATA_ DIOR	TEST _MO DE	CSPI 1_SS 0	POW ER_F AIL	CLK_ MOD E0	GPIO 1_1	WDO G_RS T	MLB_ DAT	SD2_ DATA 2	CSI_ PIXC LK	CSI_ D15	USBP HY2_ DM	USBP HY2_ DP	SD1_ CMD	VSS	Y

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.

7 Revision History

Table 87 shows the revision history of this document.

Table 87. MCIMX35 Data Sheet Revision History

Revision Number	Date	Substantive Change(s)
2	2/10/2009	• Added the following parts to Table 1, “Ordering Information”: PCIMX357CVM5B, MCIMX353CVM5B, MCIMX353DVM5B, MCIMX357CVM5B, and MCIMX357DVM5B. • Throughout consumer data sheet: Removed or updated information related to Media Local Bus interface. • Updated Section 4.3.1, “Powering Up.” • Updated values in Table 9, “MCIMX35 Power Modes.”
1	12/2008	• Updated Section 4.3.1, “Powering Up.” • Section 4.7, “Module-Level AC Electrical Specifications”: Updated NFC, SDRAM and mDDR SDRAM timing. Inserted DDR2 SDRAM timing.
0	10/2008	Initial public release

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