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Introducing Industry's Highest Performing Programmable DSP Enabling OEMs Development and Deployment of Next-Generation LTE Broadband Wireless Base Stations

PN121

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Agenda

- Emerging Broadband Wireless Standards
  - Timelines, Throughputs, and Challenges
- MSC8156 Multicore DSP
  - Block Diagram
  - Next Generation StarCore® DSP core, SC3850
  - Features and Benefits
- MSC8156 Baseband Solution
  - Target Applications
  - Development Tools
- Multicore DSP Roadmap
- Summary of Benefits
- Rules of engagement and product timelines

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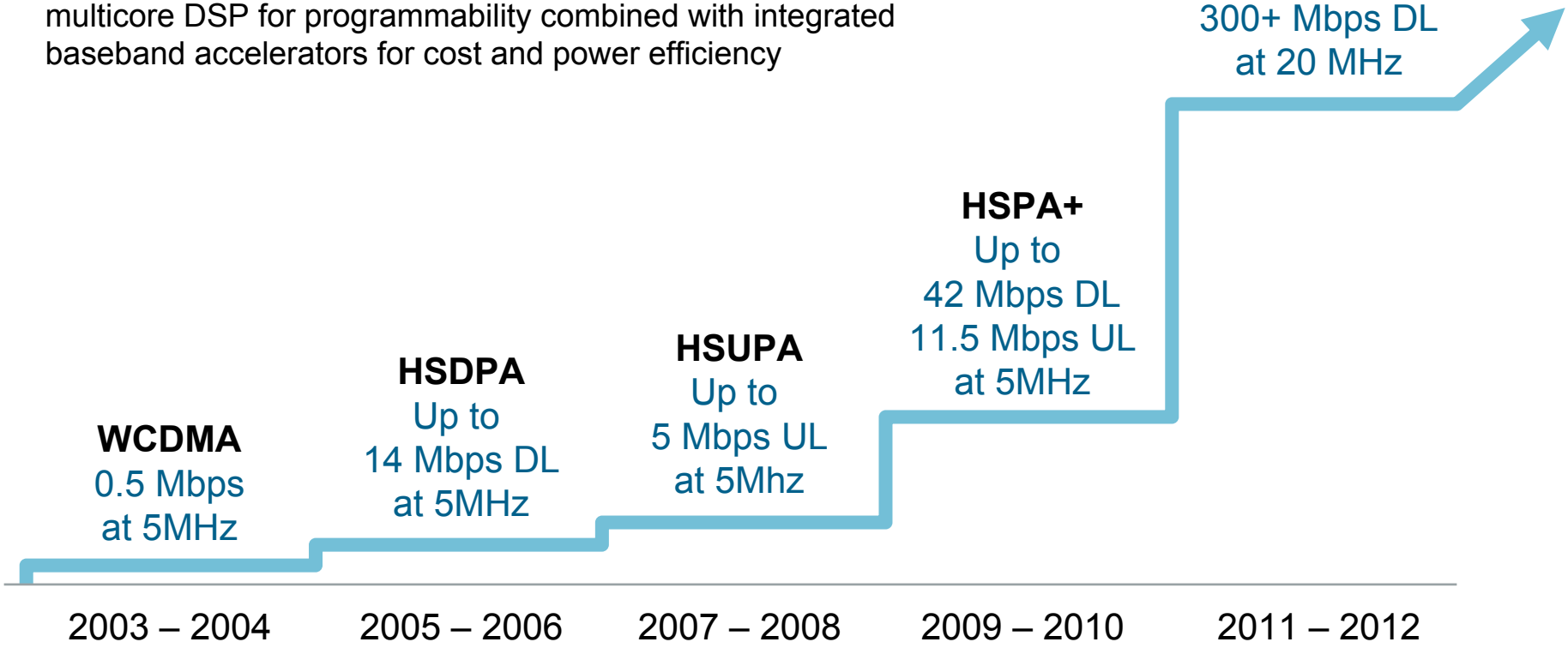
3G Evolution – from Thin to Thick Data Pipe

3G-LTE Significantly Outperforms 3G Standards

- Increasing integration for high data rates and low latencies
- Algorithm differentiation and flexibility require high-performance multicore DSP for programmability combined with integrated baseband accelerators for cost and power efficiency



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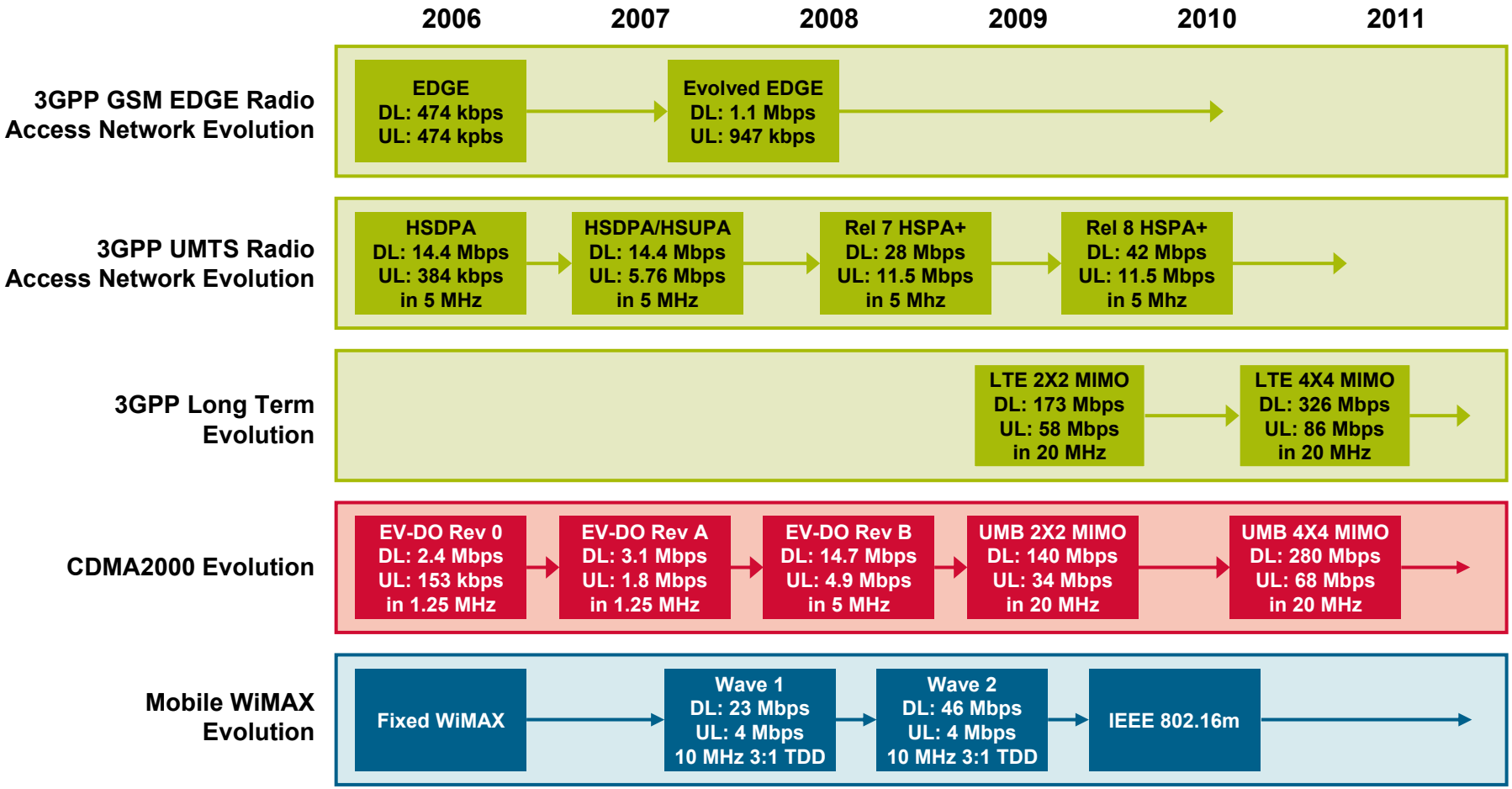
Broadband Wireless Technology Timelines



Source: Rysavy Research

Note: Throughput rates are peak network rates. Radio channel bandwidths indicated. Dates refer to initial network deployment except 2006 which shows available technologies that year.

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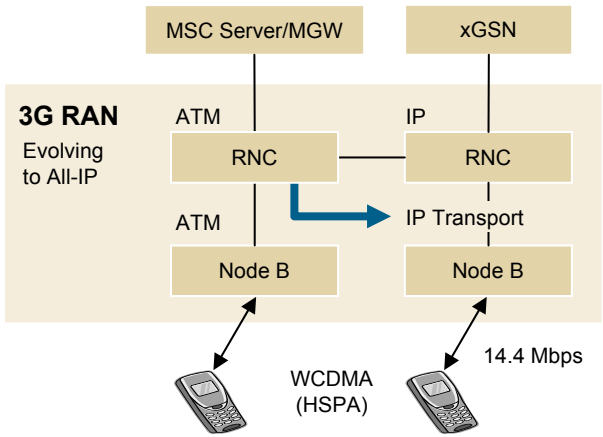
Freescale Solutions Meets 3G-LTE Challenges

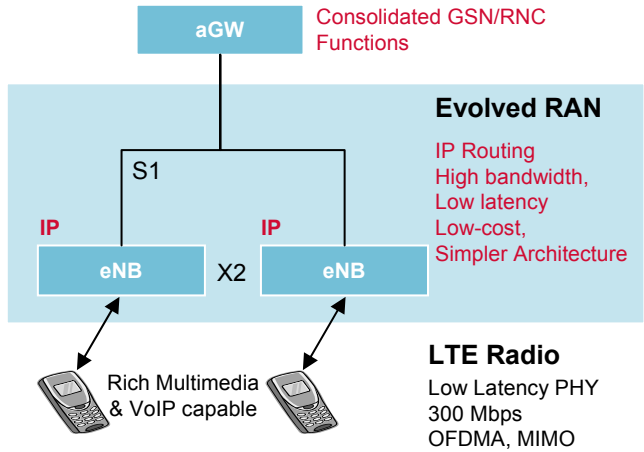
Network Evolution

3G Network



Next Generation

3G-LTE Evolved Network



Key Technology Challenges

- **High Speed Data Rate** — 100Mbps (DL), 50Mbps (UL)
- **Low Latency** — in RAN < 5ms
- **Scalable Capacity** — Spectrum Efficiency Scalable bandwidth
- **Ease of Upgrade** — reasonable OPEX/CAPEX
- **Power/Cost Optimal Architecture**
- **All IP Network** — Security
- **New RAN Architecture** — IP Routing
- **LTE Radio** — SC-FDMA (UL), OFDMA (DL) FEC, MIMO
- **Flexible Spectrum** — RF Linearity

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- **PHY Processing**
- **MAC Processing**
- **Timing Synchronization** — IEEE1588
- **High Speed Interfaces**
- **High Power RF**
- **Multicore DSP** — High Performance Platform
- **Baseband Accelerators**
- **Multicore QorIQ** — Scalable CPU Platforms
- **sRIO, PCI-Ex, GigE** — SerDES, LVDS
- **QUICCEngine, Security** — Eth. Protocols, Encryption
- **LDMOS Technology** — High Eff, Low cost package

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MSC8156 Multicore DSP

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MSC8156 Highlights

- **Target Wireless Basestation Systems**
  - 3G-LTE, TDD-LTE, WiMAX, HSPA+ and TD-SCDMA
  - Meets all leading future wireless technologies
- **Single MSC8156 Handling**
  - Single Sector 3G-LTE, TDD-LTE
  - Multi-sector WIMAX
  - Multi-carrier TD-SCDMA
  - Multi-sector HSPA along with external chip rate acceleration
- **Pioneering Expertise**
  - Leveraging multicore architecture expertise by introducing its 4th generation multicore DSP
  - First to implement Turbo/Viterbi accelerators in DSP—compliant to latest OFDMA standards
- **Highly Efficient Memory Hierarchy**
  - Large on die low latency memory:
    - 6x512KB of L2/M2 + 1MB M3 = 4Mbyte
- **MAPLE-B Accelerator**
  - Highest throughput, multi-standards compliant, re-programmable

MSC8156 Device Performance

- •Optimized Programmable Performance
  - •Based on New generation SC3850 DSP core
  - •Delivers up to 48GMACS and 6GHz effective performance
  - •Added Intelligent application specific accelerators
- •High-speed standard interfaces
  - •2xsRIO, 2xSGMII, PCI-Express
- •Highly optimized multilevel memory
- •High speed DDR3 interfaces

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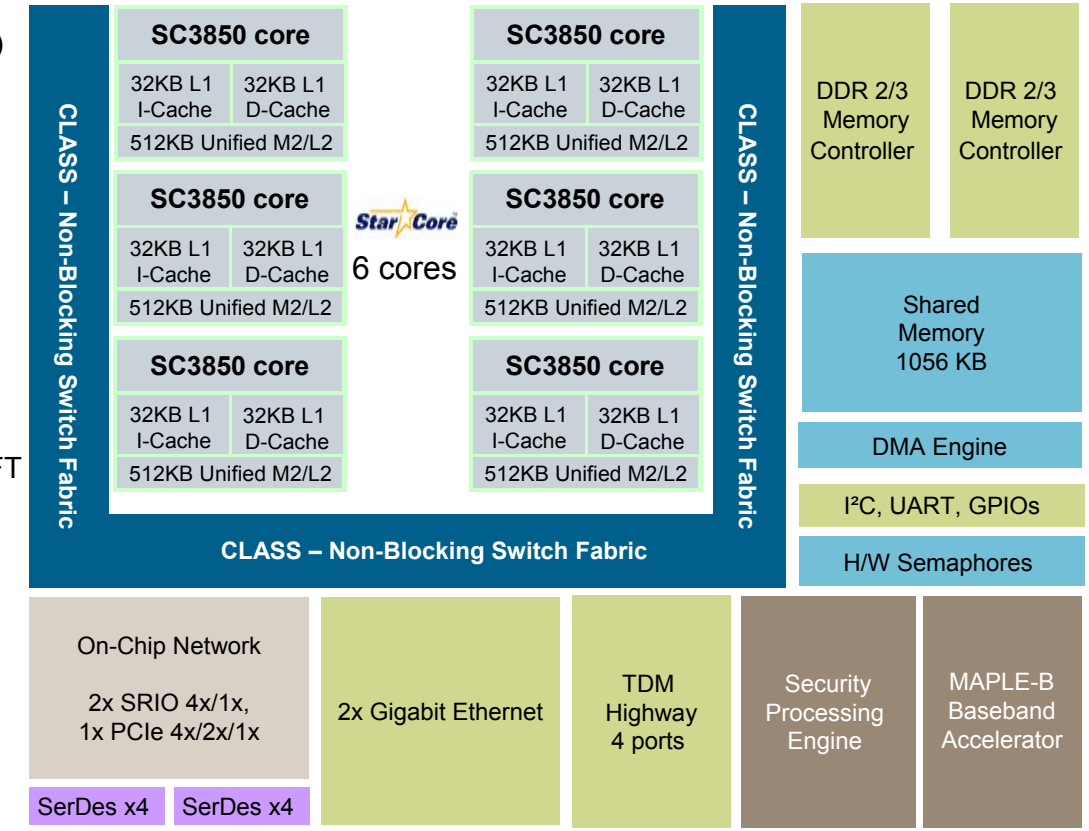
MSC8156/E – Broadband Wireless DSP

6x SC3850 Cores Subsystems (6GHz/48GMACS)

- New SC3850 DSP core at up to 1GHz (1GMACs 16b x 16b)
  - 512 Kbyte unified L2 cache or M2 memory.
  - 32 Kbyte I-cache, 32Kbyte D-cache, WBB, WTB, MMU, PIC
  - Fully Programmable
- **Internal/External Memories/Caches**
  - 1056 KByte M3 shared memory (SRAM)
  - Dual DDR3/2 64-bit interfaces at 800 MHz
- **CLASS – Chip-Level Arbitration & Switching Fabric**
  - Non-Blocking, fully pipelined, low latency
- **MAPLE-B – Baseband Accelerator**
  - Turbo/Viterbi Decoders up to 200/115 Mbps
  - FFT/DFT accelerators up to 280 Msps FFT/175 Msps DFT
  - Standards: 3G-LTE, 802.16, WCDMA, CDMA2K
- **Security Engine**
  - AES, Kasumi, SNOW-3G, SHA, RC-4 (in MSC8156E)
- **High speed Interconnects**
  - Dual 4x/1x Serial RapidIO at 1.25/2.5/3.125 Gbaud
  - PCI-e 4x/1x
- **Ethernet**
  - Dual Gigabit Ethernet ports (SGMII)
- **TDM Highway**
  - 240Mbps, divided into 4 ports of 8x E1 each.
- **DMA Engine** 32 ch memory-to-memory
- **Other Peripheral Interfaces -** SPI, UART, I2C, 32 GPIO, 16 Timers, 96KB boot ROM, JTAG



Technology

45nm, 1V core, 2.5, 1.8/1.5V I/O
FCBPGA, 29mmx29mm, 1mm pitch, RoHS

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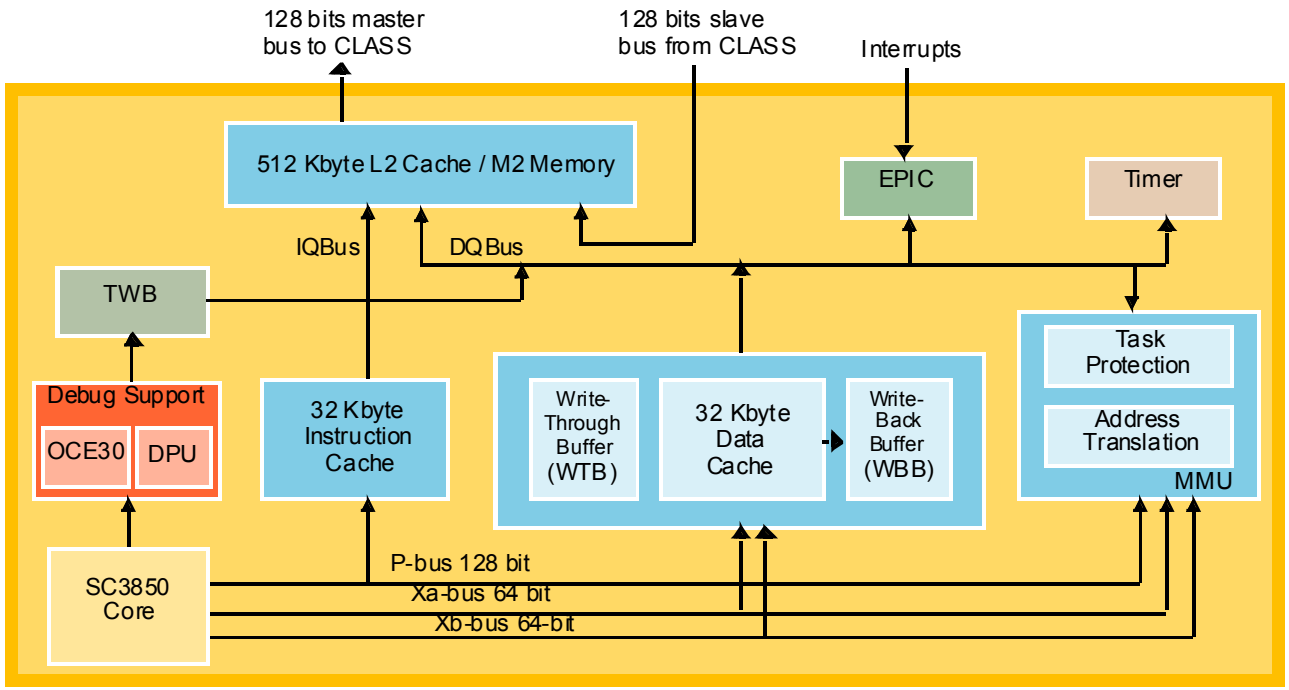
The New SC3850 Core Subsystem

- SC3850 Core DSP
- MMU
- L1 Instruction & Data cache
- Unified L2/M2 Cache
- Debugging unit
- PIC
- Timers



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New SC3850 DSP Core improvements vs. SC3400

Feature	Code Type	Highlight	Benefit
-Dual Multiply -FFT support	DSP	-Eight 16x16 multiplications per cycle -Complex operations -Mixed/Double precision MPY support -FFT dedicated ISA	-Double the throughput of convolution based kernels, complex arithmetic and mixed/double precision multiplications -Significant FFT cycle reduction with SNR increase
-Control handling ISA	CTRL	-Parallel condition computation -Pointer-Relative Accesses -AGU logic instructions -Immediate DALU register TFR -NOBTB instruction	-Accelerate decision making in control code -Faster accesses to C structures -Improved compiler support (speed and size)
-Improved µ-Arch	DSP/Ctrl	-Improved HW loop operation -Deeper speculation depth -BTB enlargement -Deeper RAS stack	-Significant control cycle improvements and a friendlier compiler target -Achieving better performance at smaller code size
-Cache support instructions	DSP/Ctrl	-DFLUSH/DSYNC, D/PFetch, DMALLOC, SWPFETCH and more… -For both L1 and L2 caches	-Improved cache operations

MSC8156/MAPLE-B Throughput & Compliance Data

Technology	Accel.	Standard Compliance	Data Rates	Comments
3G-LTE, TDD-LTE	Turbo	3G-LTE (Evolved UTRA) turbo decoding as specified in 3GPP TS 36.212, section 5.1.2.2	up to **160** Mbps (8 iterations) up to **200** Mbps (6 iterations)	Max Log Map or Linear Log Map (MAX*) Support Rate-De-Matching (sub-block de-interleaving and de-interlacing) CRC calculation
	Viterbi	3G-LTE (Evolved UTRA) channel decoding as specified in 3GPP TS 36.212, section 5.1.2.1	up to **100** Mbps (K=7 with tail biting)	Multi-iteration decoding
	FFT/DFT	FFT sizes - 128, 256, 512, 1024, 2048 points DFT sizes - Variable lengths DFT/IDFT processing of the form $2^k \cdot 3^m \cdot 5^n \cdot 12$, up to 1536 points	FFT – up to **280** Mega samples/sec DFT – up to **175** Mega samples/sec	Advanced scaling options Guard bands insertion in iFFT
	CRC	Transport and Code Block CRC for UL and DL	up to 12 Gbps	CRC check or insertion
WiMAX	Turbo	WiMAX OFDMA turbo decoding as specified in IEEE® 802.16™-2004 standard	up to **156** Mbps (8 iterations) up to **195** Mbps (6 iterations)	Max Log Map or Linear Log Map (MAX*) Support Rate-De-Matching (sub-block de-interleaving and de-interlacing)
	Viterbi	WiMAX OFDMA turbo decoding as specified in IEEE® 802.16™-2004 standard	up to **100** Mbps (K=7 with tail biting)	Multi-iteration decoding
	FFT	FFT sizes - 128, 256, 512, 1024, 2048 points	FFT2048 – up to **280** Mega samples/sec FFT1024 – up to **350** Mega samples/se	Advanced scaling options Guard bands insertion in iFFT
	CRC	PHY Burst CRC for UL and DL	up to 12 Gbps	CRC check or insertion
HSPA+	Turbo	3GPP turbo decoding as specified in 3GPP TS 25.212, section 4.2.3.2.	up to **131** Mbps (8 iterations) up to **165** Mbps (6 iterations)	Max Log Map or Linear Log Map (MAX*) Support EDCH Rate De-Matching
	Viterbi	3GPP viterbi decoding as specified in 3GPP TS 25.212, section 4.2.3.1.	up to **115** Mbps (K=9 zero tail)	
Programming Model	ALL	Buffer descriptors paradigm for allocation of data and control parameters Sharing of MAPLE-B modules in multiple devices using SRIO 'GO' command activation, no DSP core pre-processing or intervention are required		

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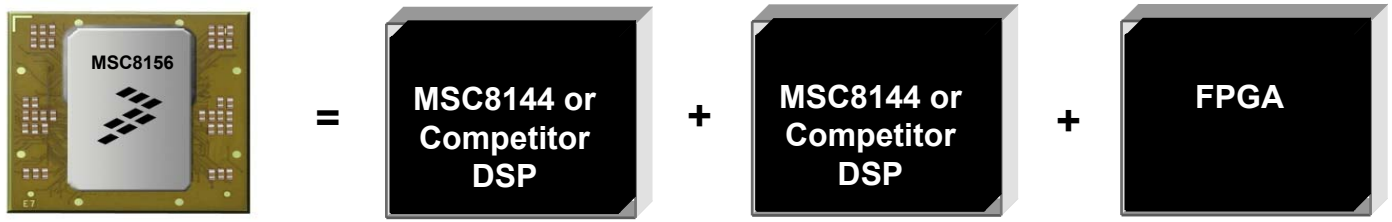
6GHZ Performance Leapfrogs Previous Generation DSPs



- 6GHz equivalent performance, 1GHz a core
- New SC3850 DSP core improves signal processing & control code performance
- Integration of high throughput and standard compliant baseband accelerators
- High throughput external interfaces and highly efficient memory hierarchy
- 45nm most advanced process technology

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Highest Performance, Multistandard DSP for Basestations

Multistandard Baseband Solution

3G-LTE Solution
20MHz 3G-LTE, 1 sector, MiMO
144Mbps downlink &
76Mbps uplink

HSPA+ Solution
Multi-sector HSPA+ *

Ready for Most Advanced Wireless Standards

3G-LTE
TDD-LTE
WiMAX
HSPA+
TD-SCDMA

No FPGA/ASIC Required

WiMAX Solution
10MHz, 3 sectors, 2Tx by
4Rx antenna single device handles
150Mbps downlink & 42 uplink

TD-SCDMA Solution
6 Carrier Basestation
handling symbol rate and
chip rate

- **Processing power equivalent to 6GHz DSP plus FPGA**
- **Based on next generation SC3850 programmable DSP core**
- **Embedded with high throughput multistandard baseband accelerators**
- **Industry's first 45nm, six core DSP ideal for infrastructure**
- **Ready for deployment of cost-optimized basestations of 3G-LTE**

* Requires an external Chip rate ASIC

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MSC8156 Value Proposition

Attributes	Features	OEM Benefits
High Performance	► Industry's highest performance programmable DSP, 6 GHz raw performance and 48GMAC 16x16 operations ► Manufactured on 45nm industry's most advanced process technology ► MAPLE-B baseband accelerator supports throughput required for 20MHz single sector 3G-LTE ► High speed interconnects dual sRIO, dual GbE and PCI-Ex ► High speed DDR3 – dual 64b 800MHz ► Highly efficient memory hierarchy with 4Mbyte of Internal memory	► Much higher densities and throughputs than previous gen. ► Effectively handles latest wireless standards requiring high speed and low latency throughput ► Cost optimized ► Enables freedom of scalability from 5MHz to 20MHz ► Single MSC8156 handles 3G-LTE 20MHz with MiMO or WiMAX 10MHz Multi sector ► Efficiently handles 3G-LTE data rates
Programmability	► MSC8156 – fully programmable DSP cores ► MAPLE-B accelerators supports latest wireless standards and consists of pre-configured and re-programmable RISC engines	► Enables integrating OEM's intellectual property using highly efficient compiler and tools ► Enables designing of unified, upgradable, standard compliant and multistandard basestations
Efficiency	► FPGA-less PHY solution, development of FPGA or ASIC is not required ► Ultra-efficient DSP specifically designed to handle the computationally intensive processing of baseband requirements of LTE data bandwidth ► Industry standard high speed interfaces ► Low power solution	► Expedite time to market and reduce development costs ► Significant lower cost channel card ► Reduced development effort, power consumption and cost-effectiveness play key factors in basestation design ► Enable daisy-chaining of sRIO eliminating the need for sRIO switch ► Efficient board routing
Upgradability and Compatibility	► Safe roadmap continuum for new DSP cores, DSP devices and process technologies ► "C" base language portable and upgradable solutions from existing products ► Binary code compatibility from one generation to another	► Freedom to change from legacy silicon vendors ► Enable seamless transition to next generation devices ► Provides the opportunity to take full advantage of LTE capabilities today

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Ideal for 3G-LTE & WiMAX Basestations

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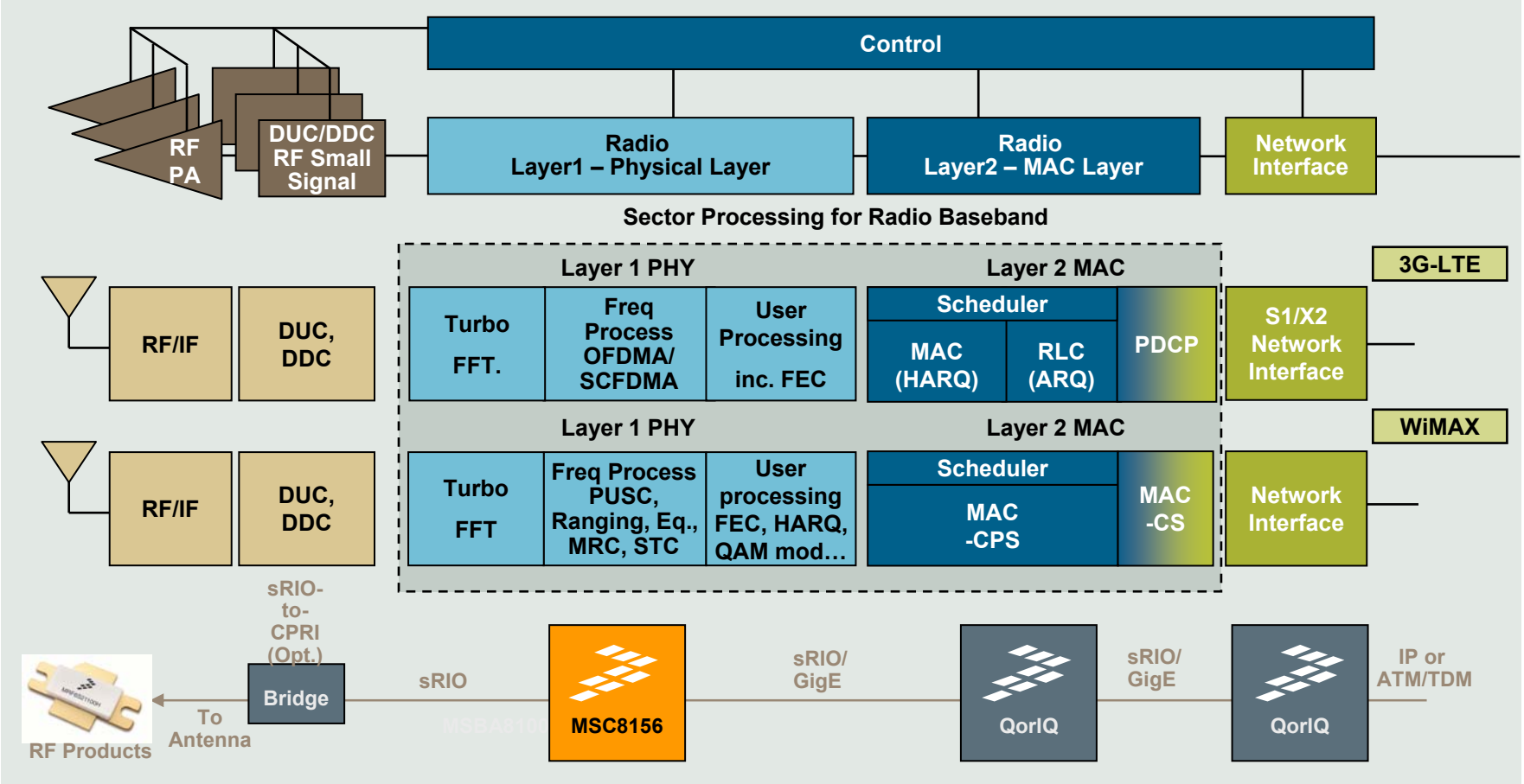
MSC8156 in 3G-LTE & WiMAX Processing Chain



- Layer 1 - PHY, Layer 2 - MAC
- No FPGA/ASIC required
- Scalable platform

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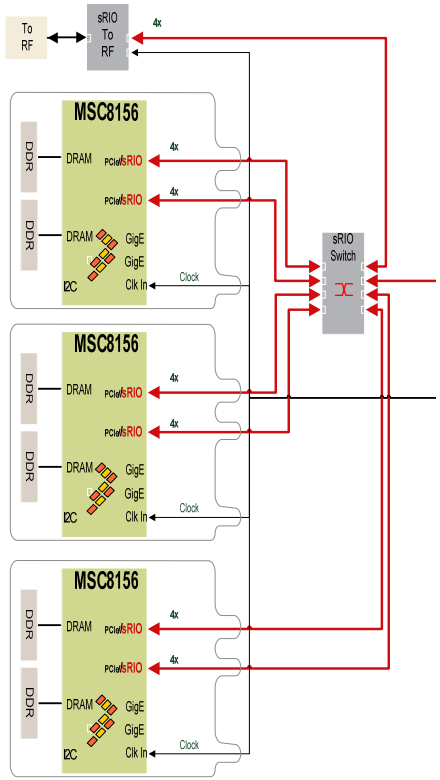
3G-LTE, 20 MHz FDD, 3 Sectors – Layer 1 Architecture



Scalable Solution

- Covers configurations up to 20 MHz, 430Mbps downlink & 230Mbps uplink,1 carrier/3 sectors, with 4Tx and 4Rx antenna
- Each MSC8156 DSP covers PHY handling uplink and downlink for 1 sector
- Separate Serial RapidIO® connection for both data and control paths

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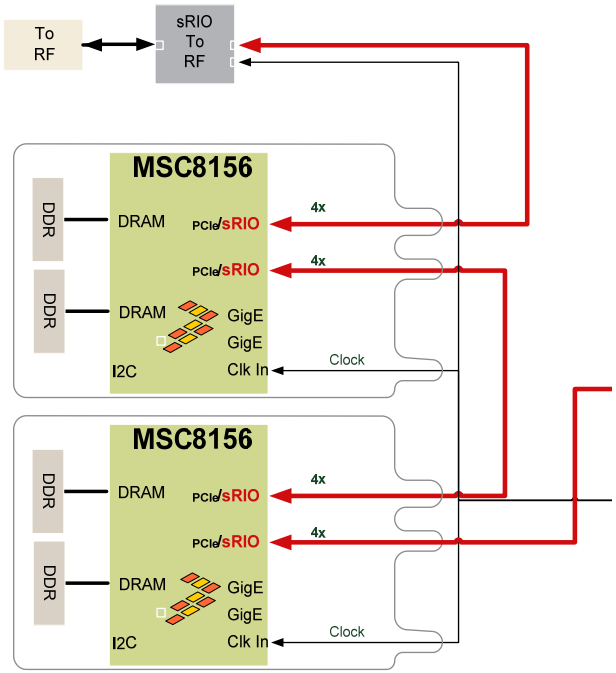
WiMAX 802.16e, 10 MHz TDD, 3 Sector – Layer 1 Architecture



Scalable Solution

- Covers configurations up to 10 MHz, 300Mbps downlink & 42Mbps uplink,1 carrier with 3 sectors, with 4Tx and 8Rx antenna and beamforming
- Allows for direct connectivity to the backplane and antenna without a switch by daisy-chaining Serial RapidIO®

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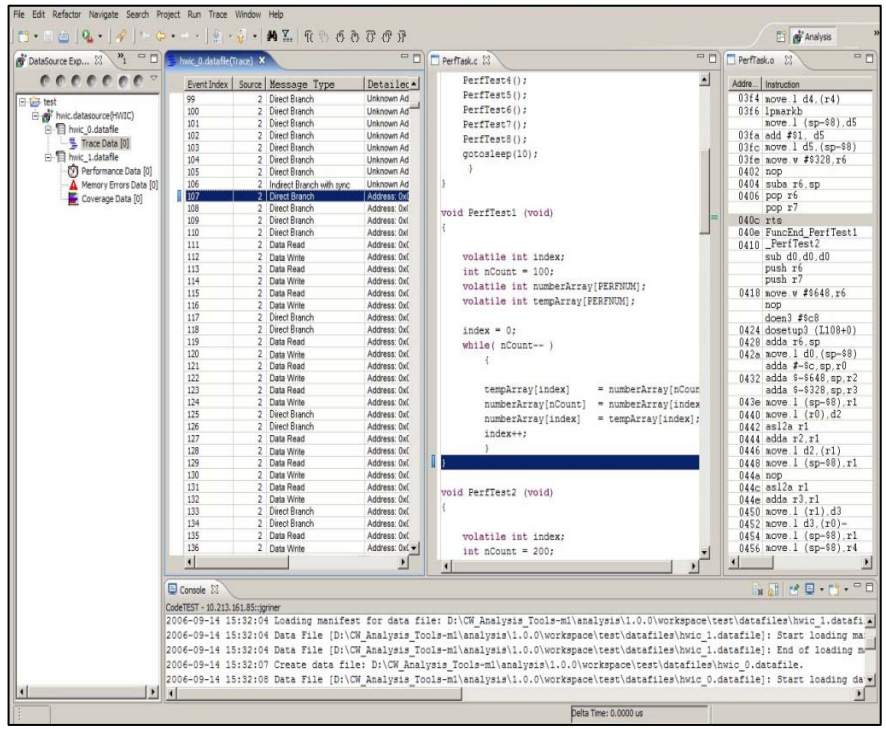
MSC8156 Easy to Use Development Tools – CodeWarrior 10.x

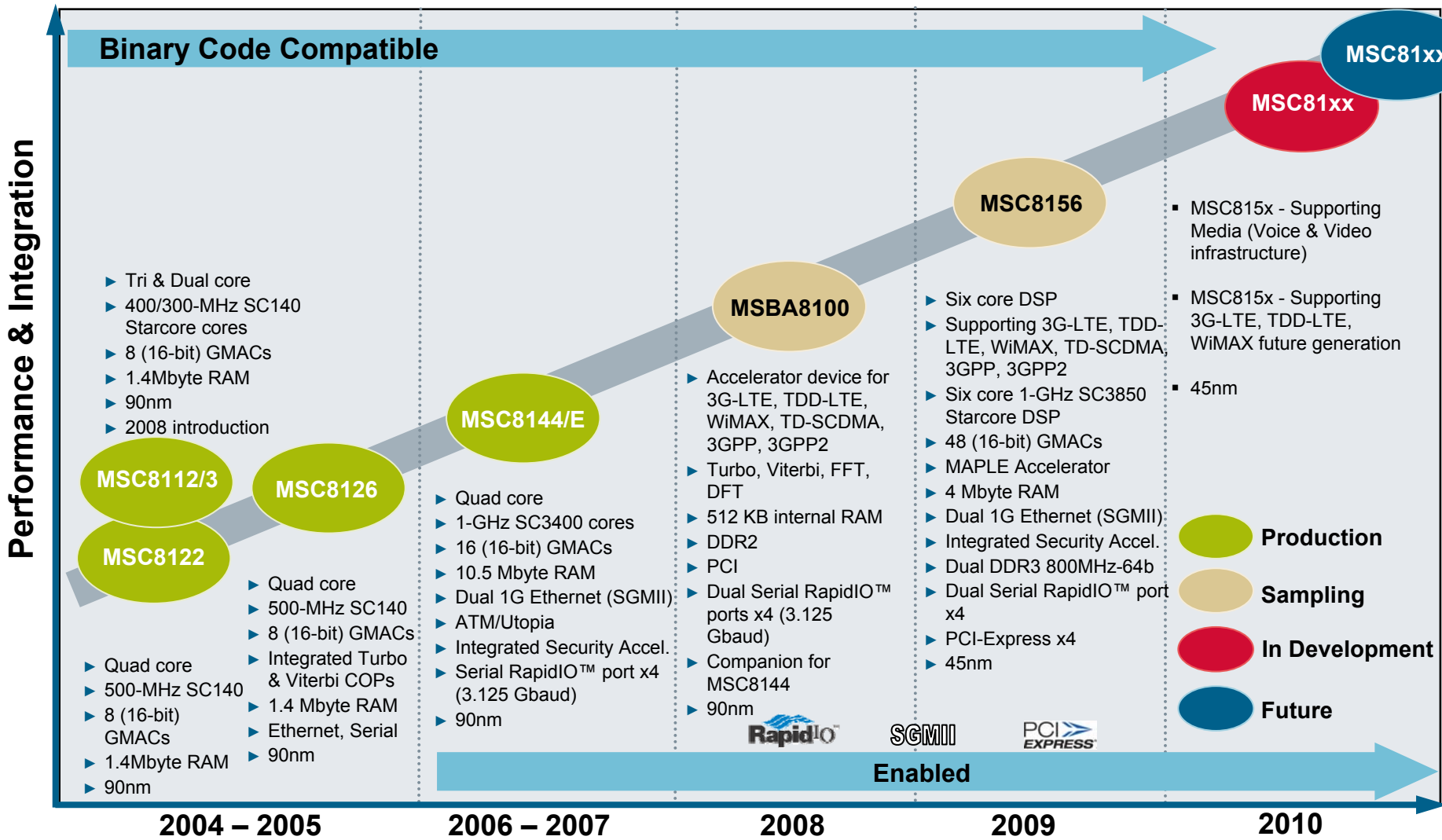
- **CodeWarrior® IDE**
  - Eclipse-based
- **StarCore® Build Tools**
  - ‘C’ & ‘C++’ Optimizing Compliers, Linker, ASM, Utilities
- **Debugger**
  - Multicore and Multi-DSP support
  - Full access and control
  - USB and Ethernet TAP probes for silicon debug
- **Trace & Profile**
  - Support of advanced debug & profiling capabilities/analysis
  - MSC8156 silicon & simulator targets
- **Software Simulators**
  - Core Platform Cycle Accurate
  - Device Functional Accurate
- **SmartDSP-OS RTOS**
  - Field deployed
  - Fully pre-emptive
  - Royalty free
  - Built-in device drivers for MAPLE-B, Serial RapidIO, Eth, TDM, DMA, SPI, I2C



Development Board

- Includes MSC8156 device

Multicore StarCore® DSP Roadmap



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MSC8156 Summary

- OEMs can take full advantage of LTE capabilities today
  - 6 GHz raw performance with fully programmable cores
  - Embedded Freescale MAPLE-B technology that accelerates Turbo and Viterbi decoding, Fast Fourier Transform (FFT), Inverse Fast Fourier Transform (IFFT), Discrete Fourier Transform (DFT), and Inverse Discrete Fourier Transform (IDFT) — operations currently performed in FPGA or custom ASIC devices
  - Contains two configurable RISC engines, can be reprogrammed to accommodate updates
  - Supports legacy 3G technologies as well as the newest wireless standards — the same DSP can be used for multiple technologies or in a multistandard basestations
- Manufactured in 45nm process technology
  - Significantly increases performance and design energy efficient solution while integrating more functionality
  - More cost effective solution, to design small form factor channel cards that take up less space, increased functionality and consumes less power giving the opportunity to provide differentiated and competitive solutions for their customers
- Reduces chip count and eliminates the need to attach costly, customized and power hungry dedicated devices
  - The combination of 6 cores DSP plus baseband accelerator into a single SoC can be used for final and cost optimized system production

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Additional Information

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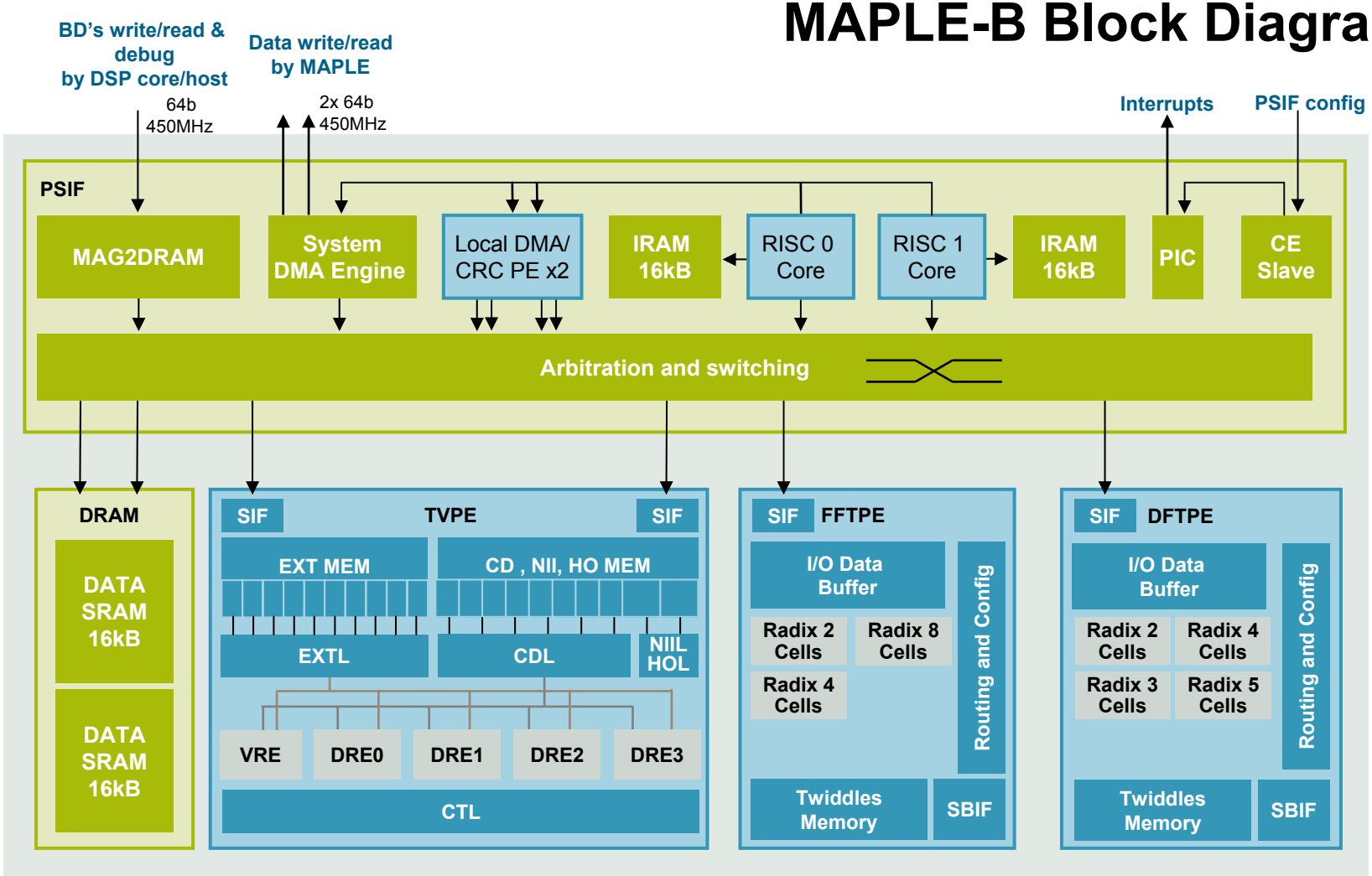
MAPLE-B Block Diagram



PSIF : Programmable System Interface
TVPE : Turbo/Viterbi Processing Engine
FFTPE : FFT Processing Engine
DFTPE : DFT Processing Engine

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Pedestal ID	Demo Title