



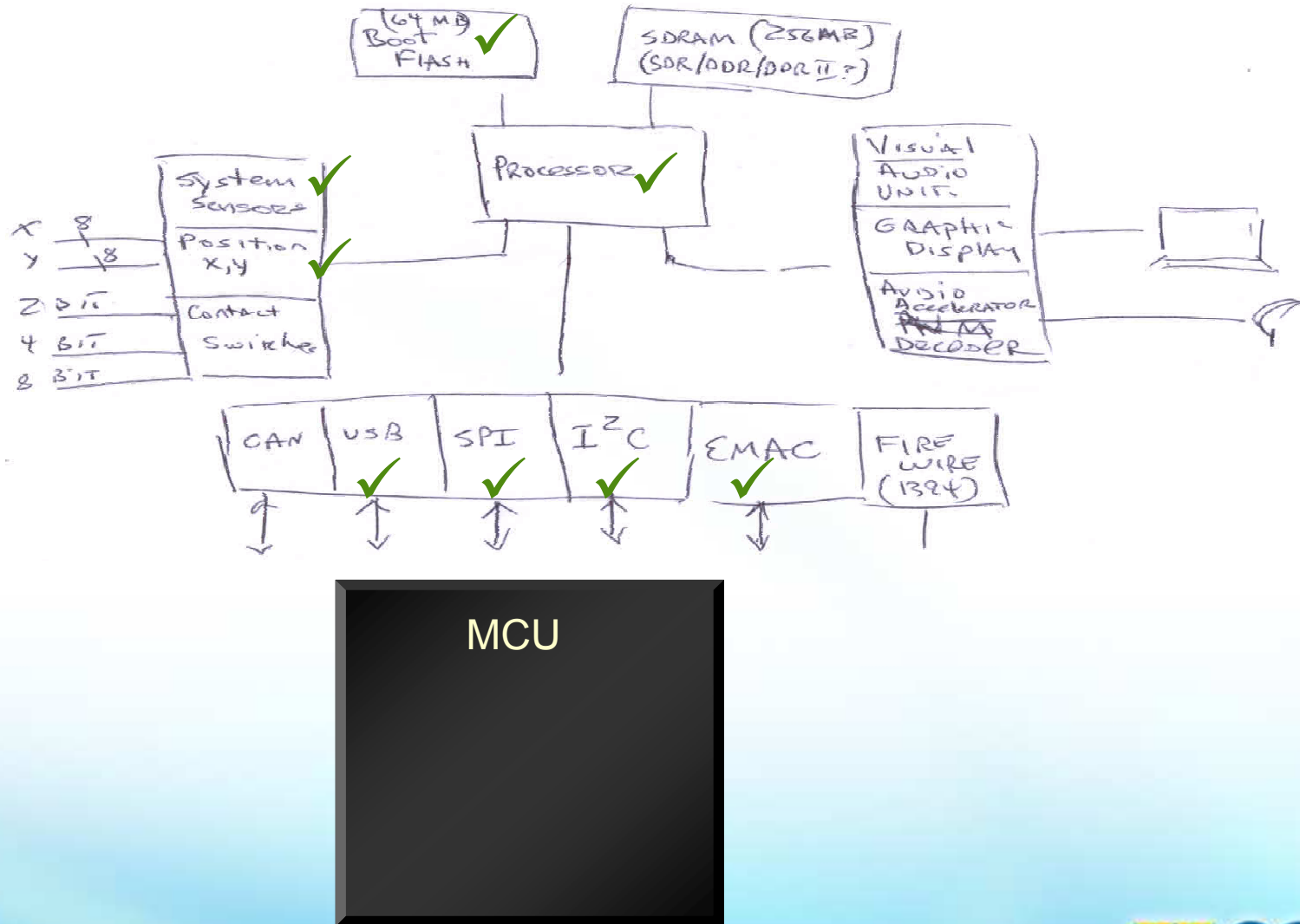
使用**Altera**嵌入式解决方案，
提高性能，降低功耗

ALTERA®

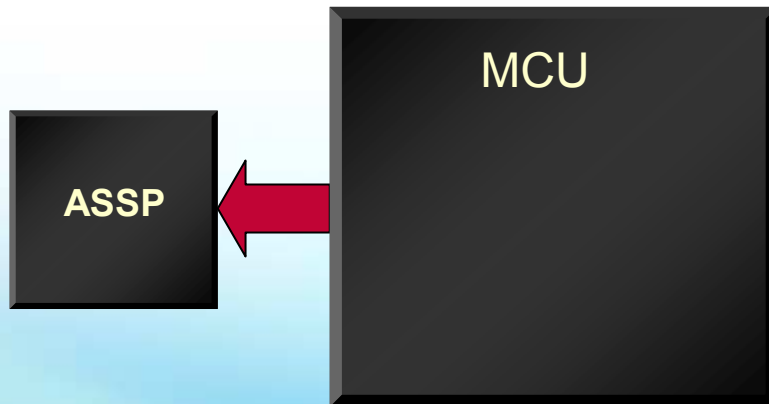
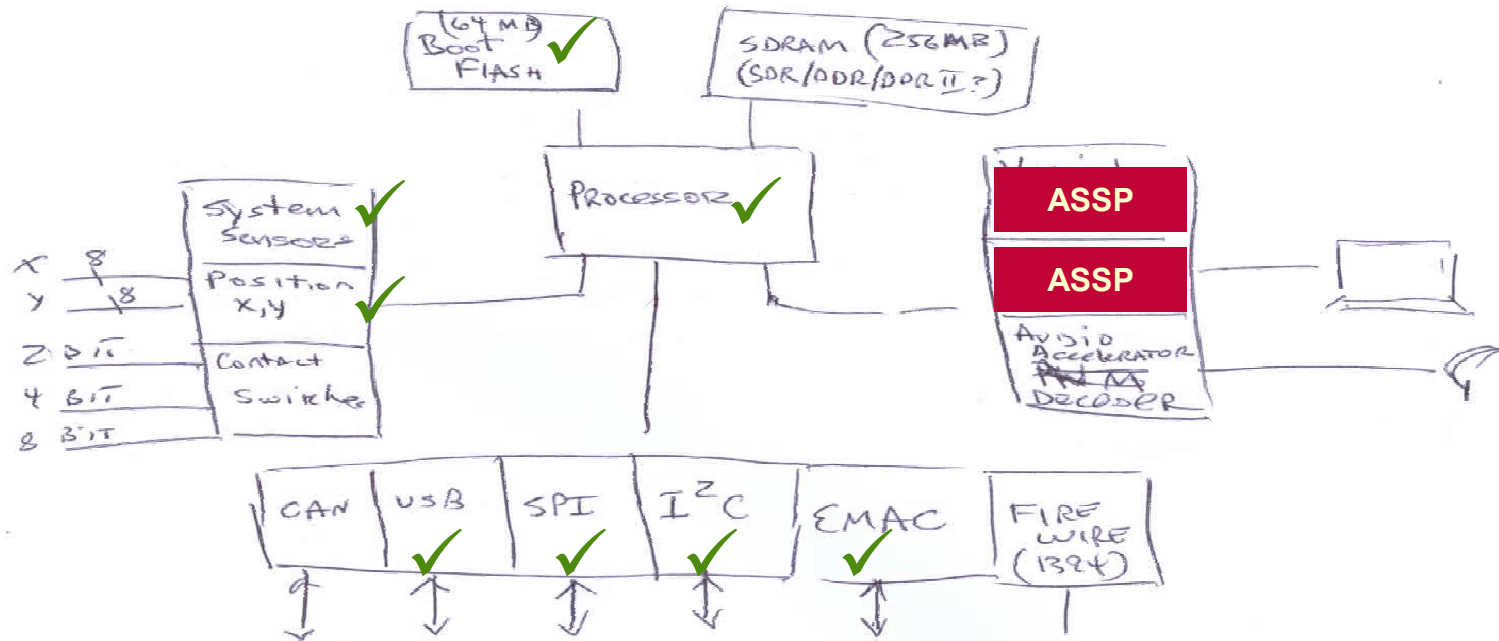
议程

- 什么是**Altera**嵌入式解决方案？
- **Nios**嵌入式评估套件：演示
- 提高性能，降低功耗
- 资源
- 总结

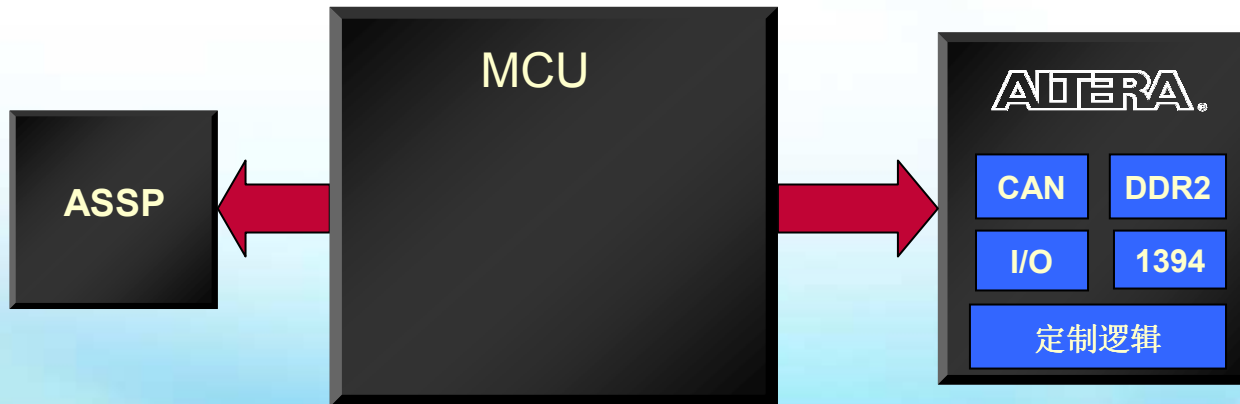
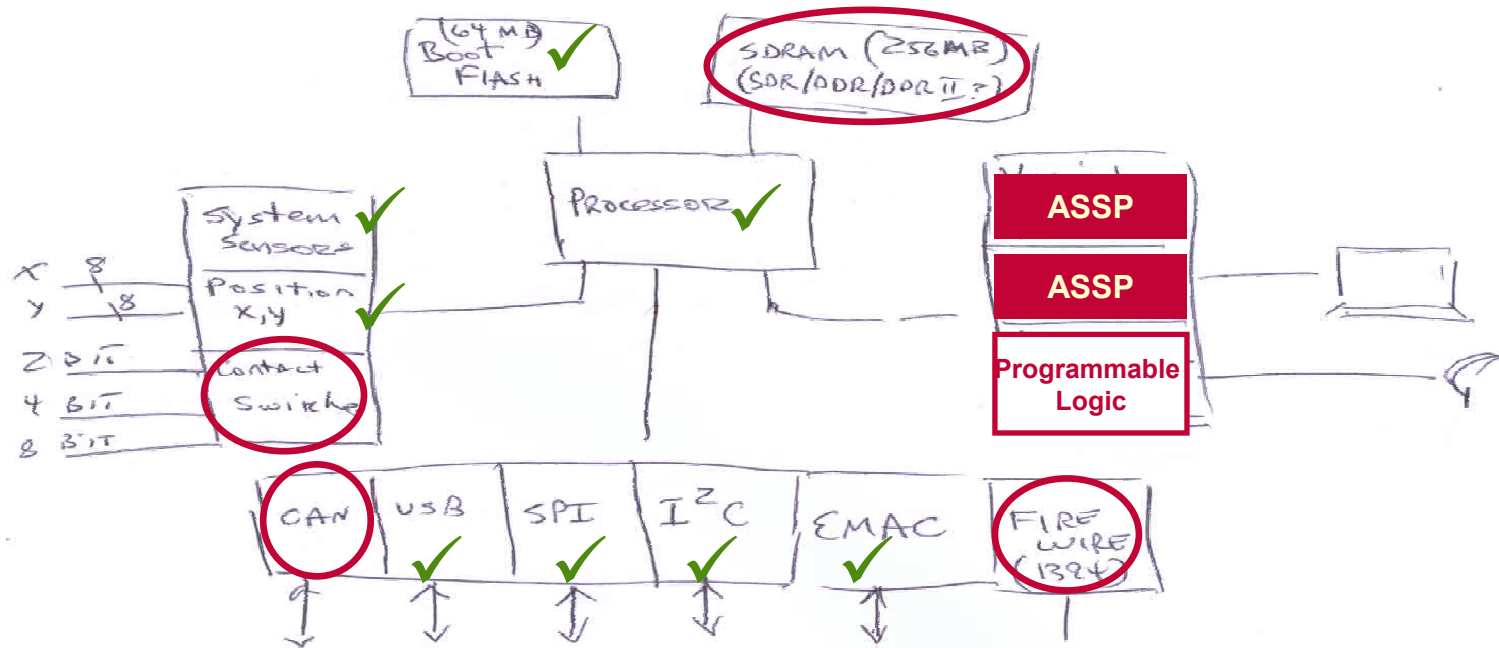
传统的(多芯片)系统



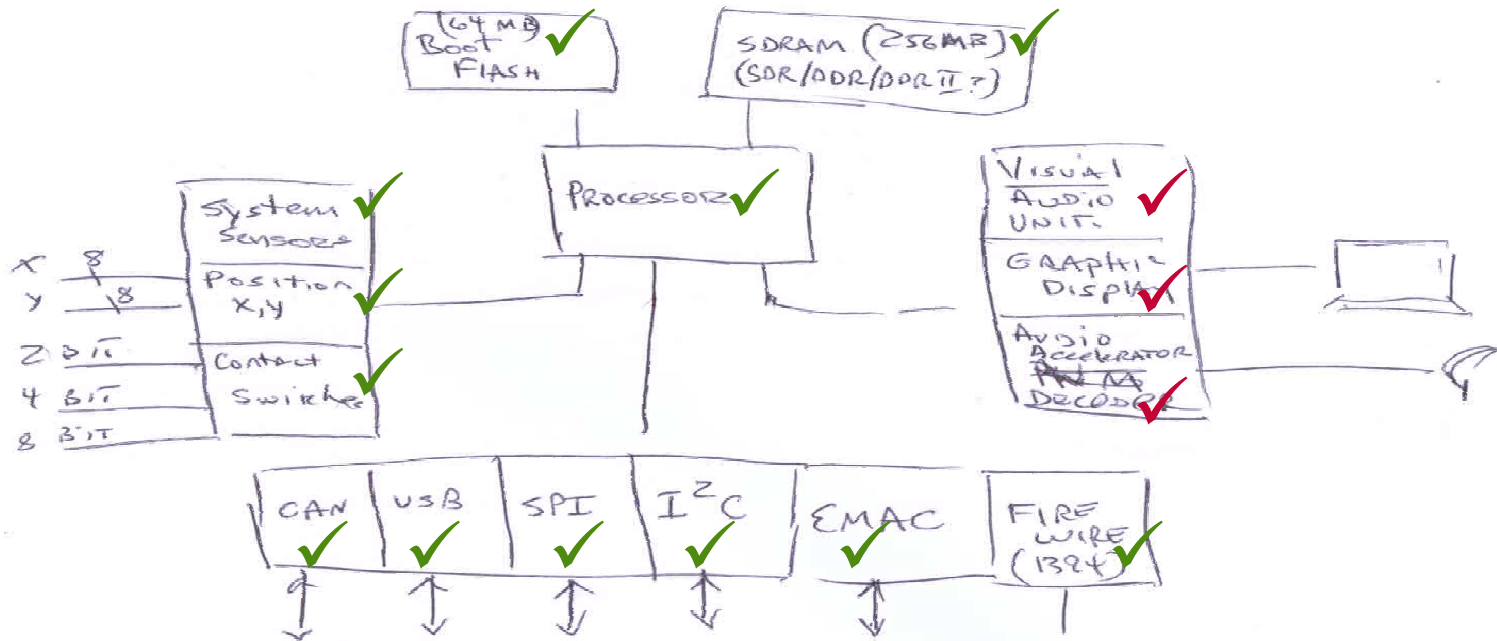
传统的(多芯片)系统



传统的(多芯片)系统



可编程芯片系统(SOPC)解决方案



ALTERA		
图形引擎	CPU	VGA
闪存控制器	EMAC	CAN
DDR2 控制器	IIC	1394
SDRAM 控制器	SPI	USB
Custom Logic		

- 最合适解决方案
- 降低了系统成本
- 降低了系统功耗
- 不会过时

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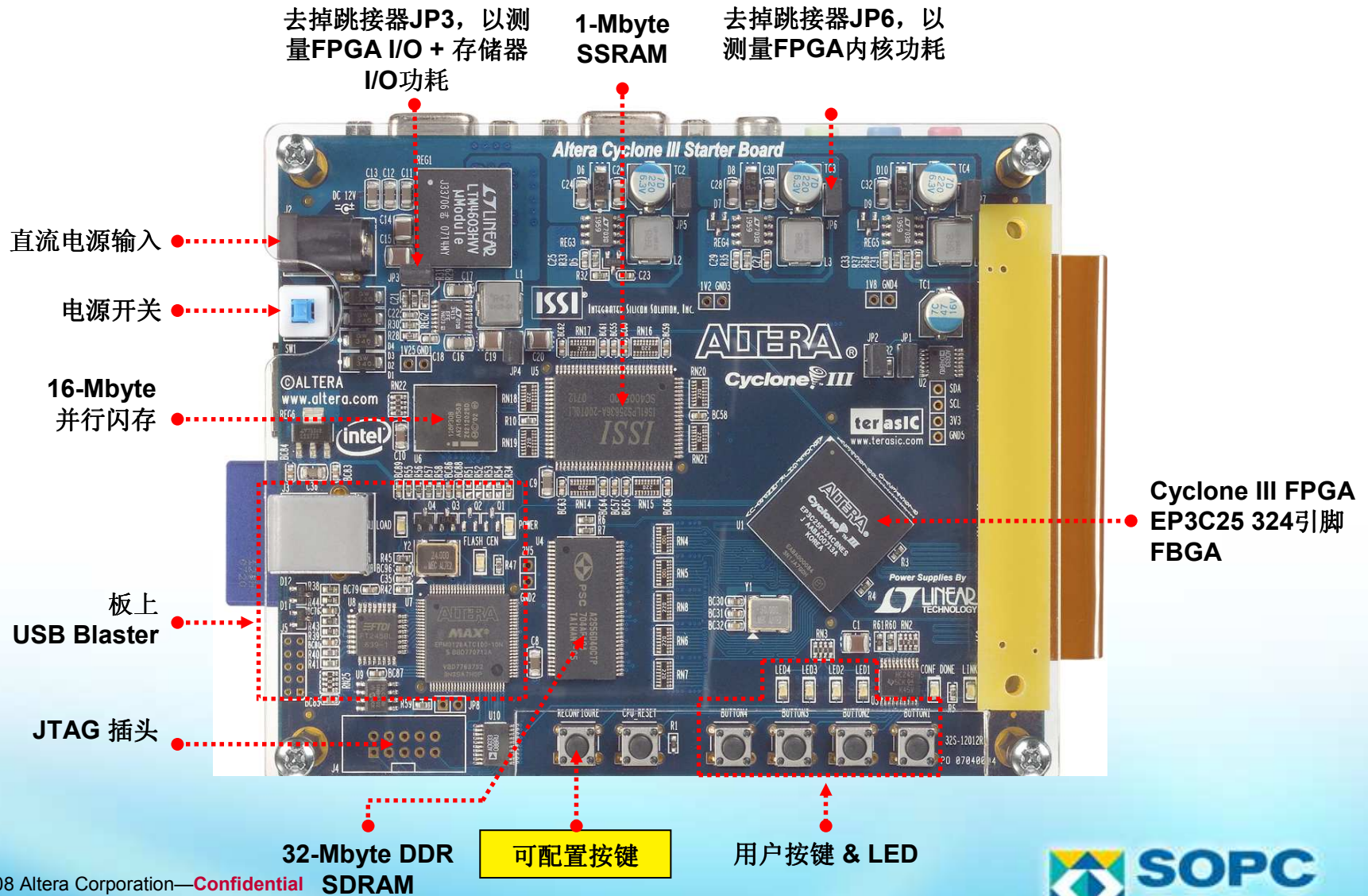




Nios嵌入式评估套件： 演示

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Cyclone III FPGA基本板



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32-Mbyte DDR SDRAM

可配置按键

用户按键 & LED



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LCD多媒体子卡

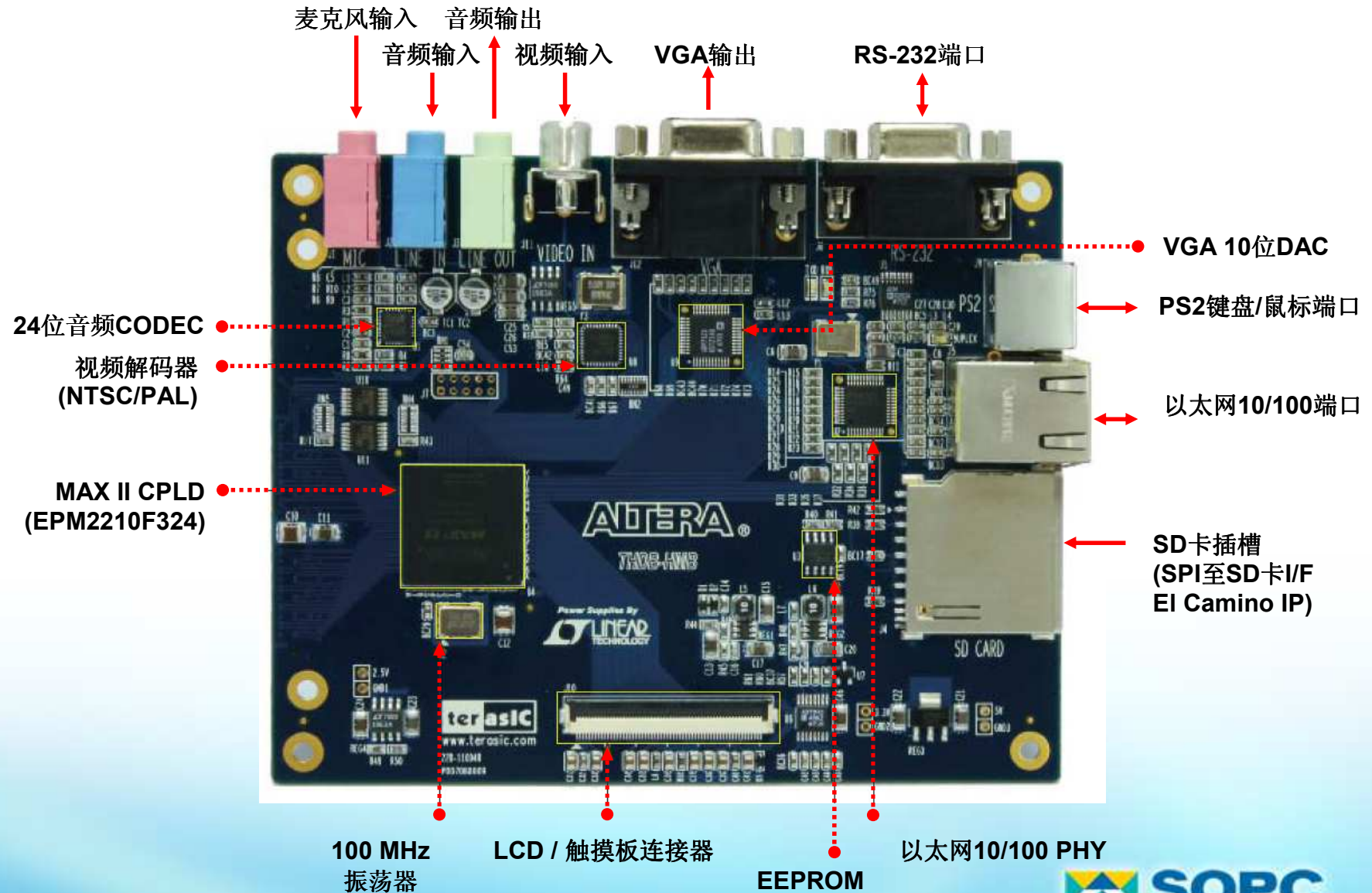


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LCD多媒体子卡(去掉了LCD)

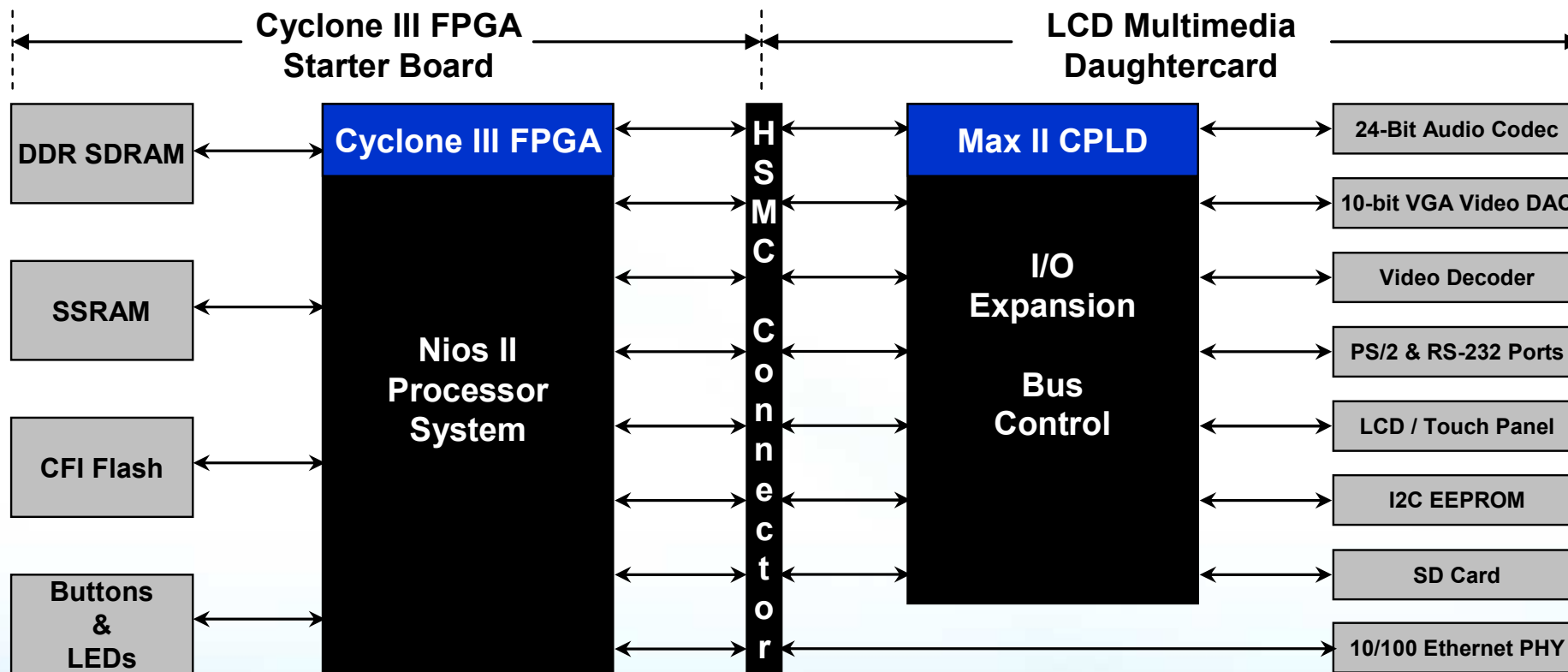


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系统级框图



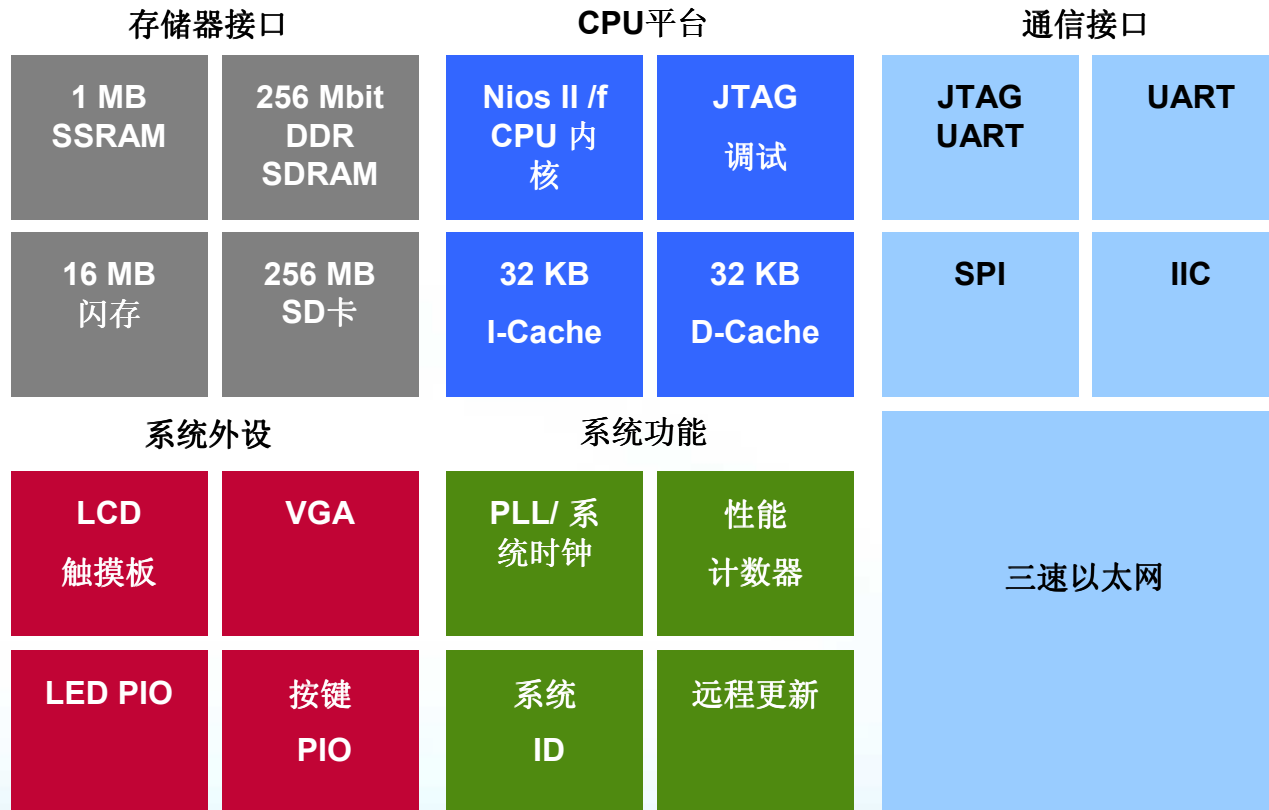
Max II EPM2210F324器件用于I/O扩展、电压转换，以及在EEPROM中存储MAC ID。

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Nios II标准处理器系统



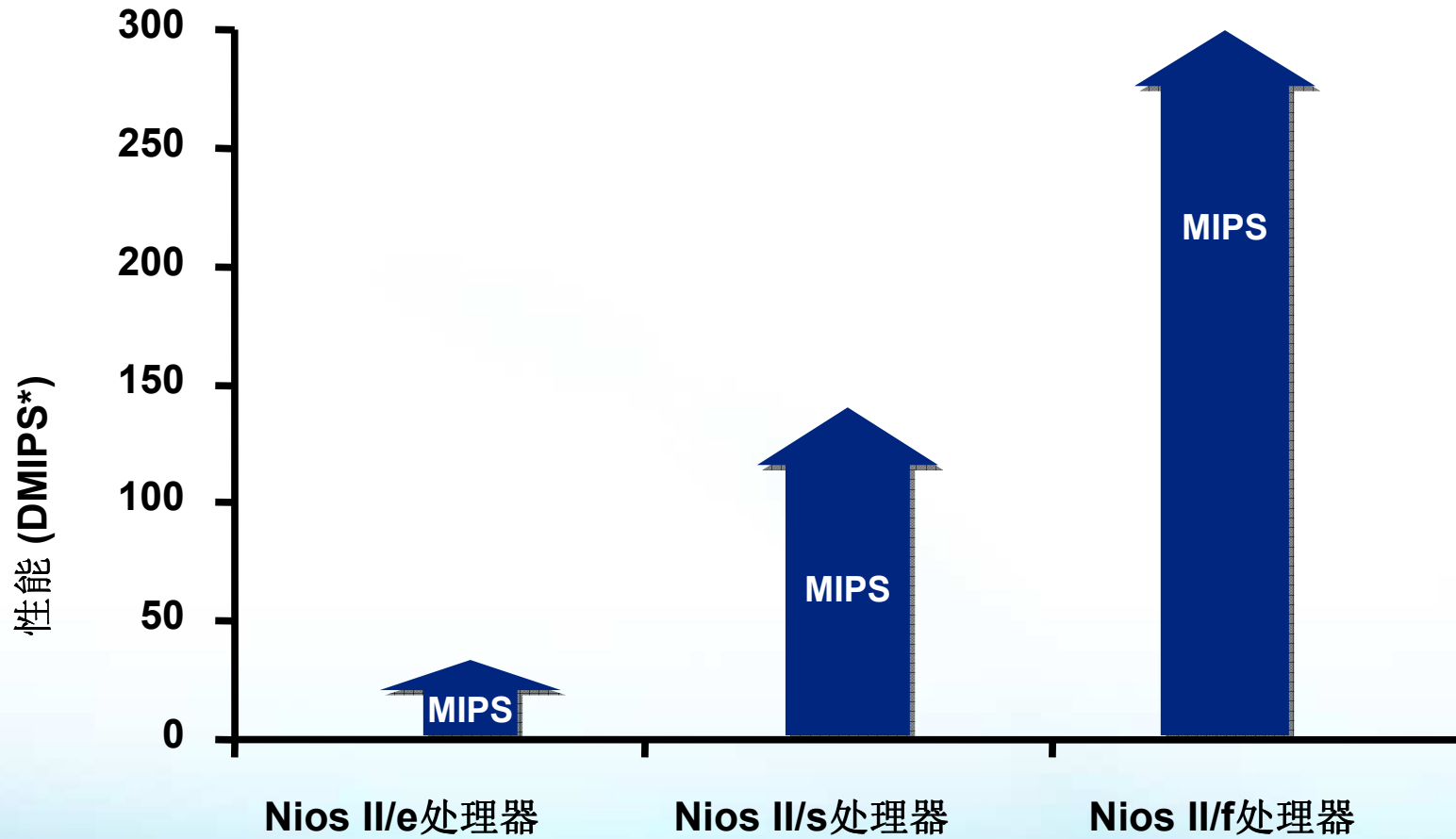
使用了**18 K**逻辑单元, **175 K-bits**存储器



提高性能，降低功耗

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性能范围



* Dhrystone 2.1基准测试



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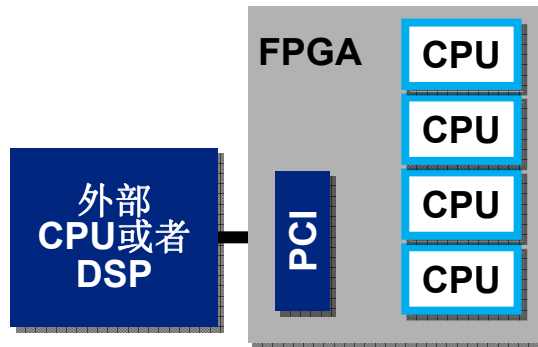
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Nios II处理器性能 (DMIPS)

器件系列	Nios II/f 处理器	Nios II/s 处理器	Nios II/e 处理器
Stratix III FPGA	300	128	50
Stratix II FPGA	251	110	44
Stratix FPGA	168	82	27
Hardcopy® Stratix II	228	129	49
Hardcopy Stratix	166	84	27
Cyclone III FPGA	165	68	17
Cyclone II FPGA	144	55	18
Cyclone FPGA	130	53	17

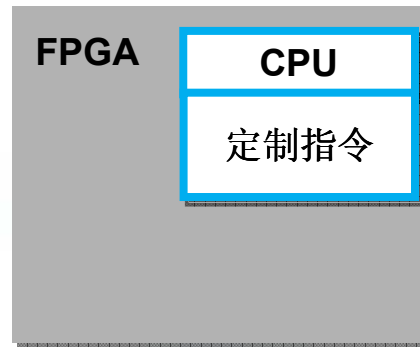
提高性能的3种方法

多处理器系统



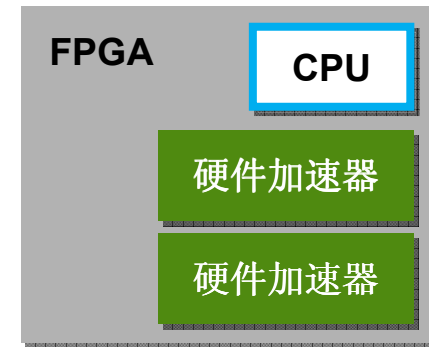
- 加入处理器
(内部以及外部)

定制指令



- 加速每个CPU的性能(加入专用指令)

硬件加速器

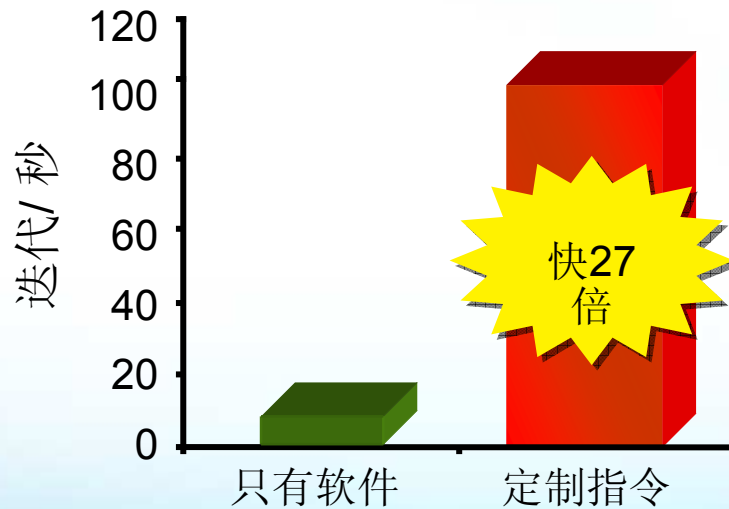


- 通过专用硬件加速变换算法

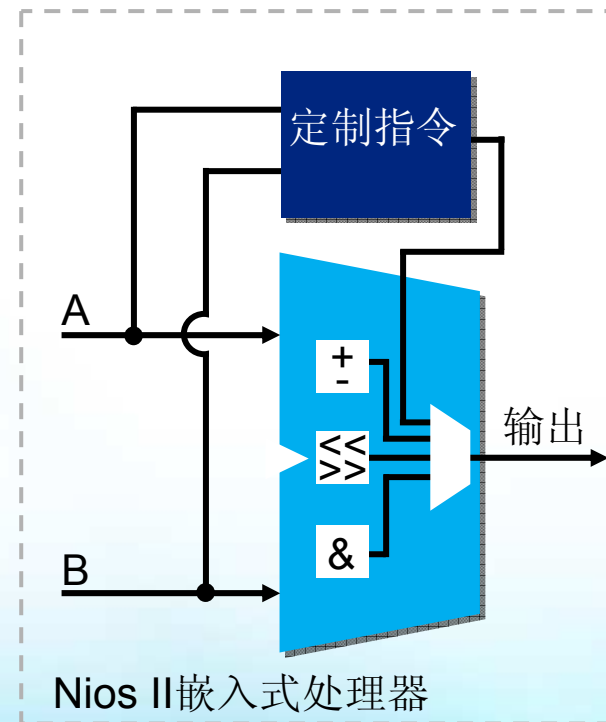
定制指令

■ 扩展CPU性能

- CPU获取数据，存储结果
- 适合数学和逻辑运算
 - 例如，浮点，位处理
- 硬件要比软件快得多



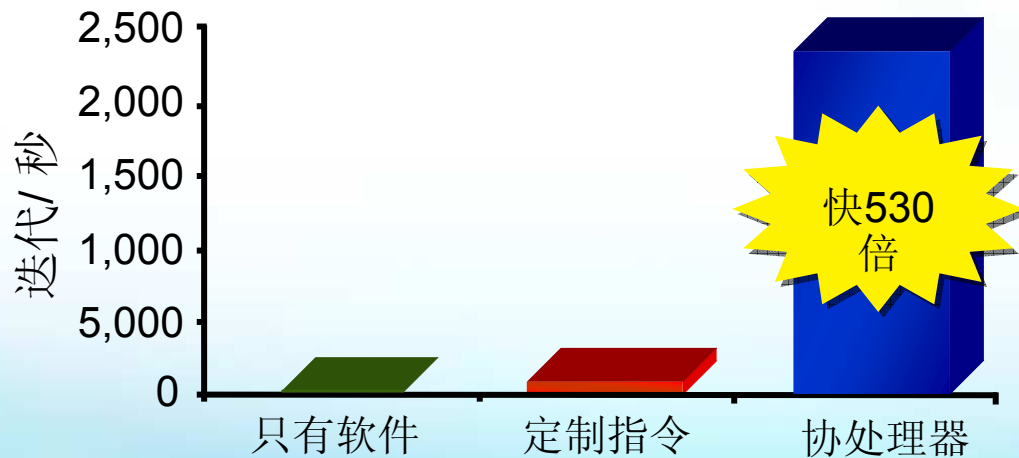
* 例子: CRC 64kbyte缓冲



硬件加速器

■ 并发数据协处理器

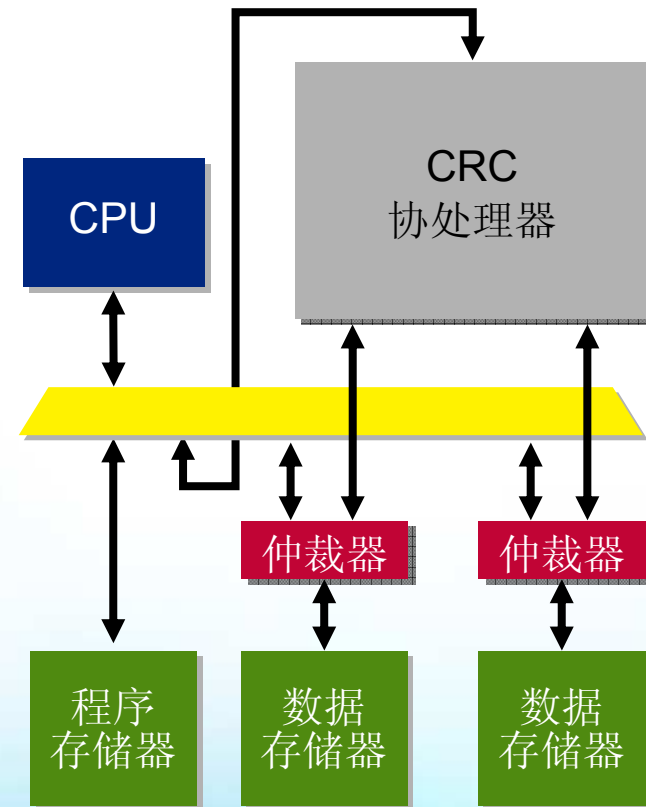
- CPU启动/停止协处理器
- 协处理器获取数据，存储结果
- CPU同时运行应用程序代码
- 适合大块数据运算



* 例子: CRC 64kbyte缓冲

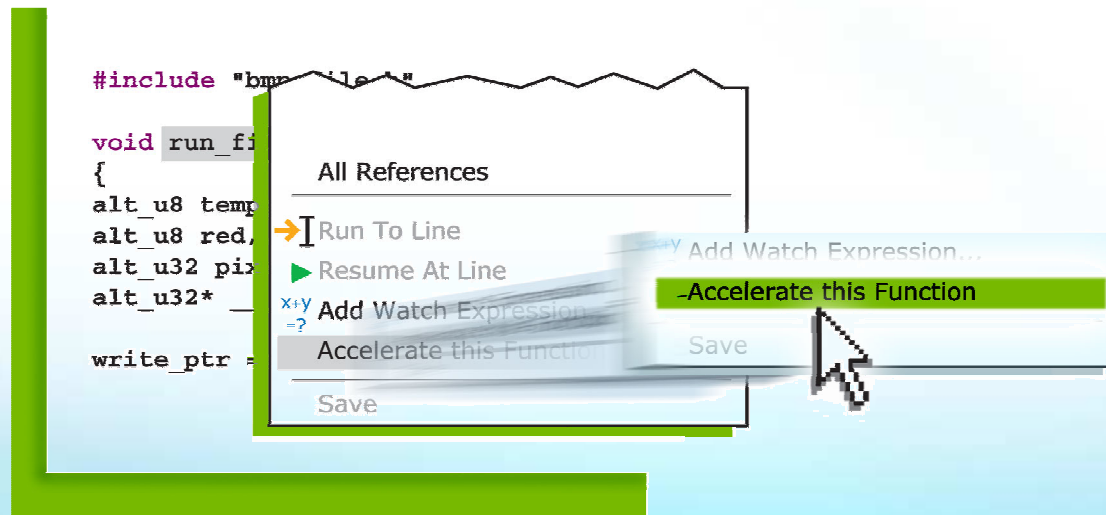
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Nios II C语言至硬件加速编译器

- 自动建立并集成硬件加速器
- 直观的用户界面，简化了C语言加速。
- 使用熟悉的Nios II IDE
- 支持标准ANSI C语言

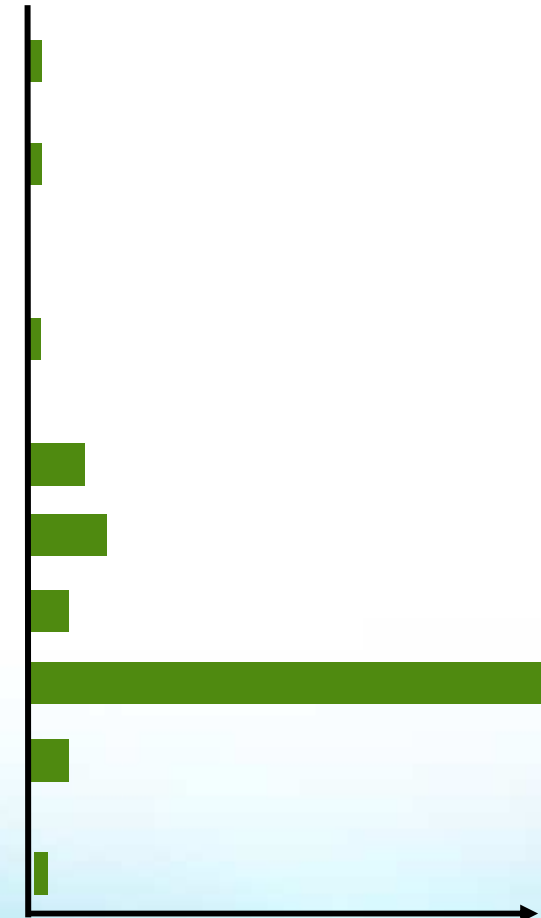


右键单击加速

C语言至硬件加速

```
main ()
{ ...variable declarations...
  init();

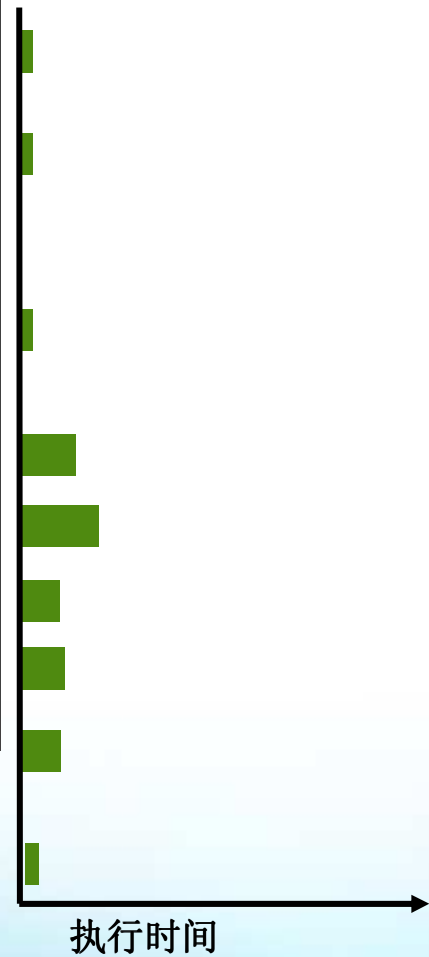
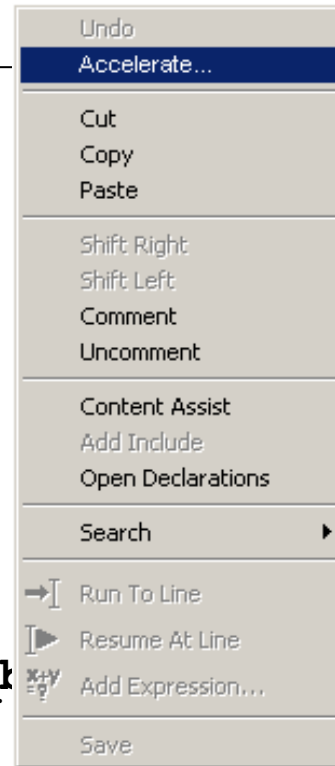
  while (!error && got_data())
  {
    do_user_interface();
    gather_statistics();
    if (got_new_data())
      d_transform(in_buf, out_buf);
    check_for_errors();
  }
  cleanup();
}
```



右键单击加速实现函数功能

```
main ()
{ ..variable declarations...
  init();

  while (!error && got_data())
  {
    do_user_interface();
    gather_statistics();
    if (got new data())
      d_transform in_buf, out_buf;
    check_for_errors();
  }
  cleanup();
}
```



系统功耗



- 去掉分立处理器，降低功耗。
 - “... 我们的元件成本至少降低了20%，而功耗则是以前的五分之一。”

-David Main, 工程组经理

- 以1/5的功耗将性能提高5倍 (C2H)

- AN531: 采用硬件加速降低功耗
- 下载设计实例

Introduction

Reducing power consumption in embedded products that use FPGAs is increasingly important, particularly for battery-powered applications or to reduce heat or cost. You can use parallel algorithms to exploit the parallel architecture of FPGA devices to accomplish more work per clock cycle, allowing you to lower the clock frequency. High-level development tools such as SOPC Builder and the Nios® II C-to-Hardware Acceleration Compiler (C2H) can help you use the power-saving potential of the FPGA hardware by easily adding hardware accelerators and lowering clock frequencies.

Basics of Power

There are two essential components to the power consumption of a CMOS device: static power and dynamic power.

Static Power Versus Dynamic Power

Static power, sometimes also called leakage current or standby current, is the power consumed as a result of current that leaks through a device's transistors while they are static. Because static power is a relatively constant characteristic of a particular device, there is little you can do in an FPGA design to reduce the static power consumption, except to use a smaller FPGA device.

Dynamic power is the power consumed as a result of the current that flows through transistors as they switch states. In digital CMOS circuits, this transition time is when most current flows through the transistors; therefore, this is when the transistors consume the most power. In a synchronous digital CMOS circuit, most power is consumed during clock transitions, so higher clock frequencies usually translate to higher power consumption. One key to reducing power consumption is clocking the logic as infrequently as possible.

Because dynamic power is highly dependent on the clock frequency, you can potentially reduce the amount of dynamic power that an FPGA design consumes by parallelizing some of the application's tasks so that more work is done per clock cycle, thereby lowering the clock rate. The total power is only reduced if the power saved by reducing the clock rate is greater than the power consumed by the additional logic required to parallelize the task.

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Reducing Power in Embedded Systems by Adding Hardware Accelerators

By Rodney Frazer
Embedded.com
(04/09/08, 03:21:00 PM EDT)

The rule of thumb in embedded system design has been that adding hardware increases power demands. The careful use of hardware accelerators, however, inverts the rule: adding hardware can reduce power.

By analyzing algorithms and implementing appropriate accelerators in programmable logic, developers can increase a design's performance while reducing power consumption in an embedded computing system.

Table 2: Effect of Reducing Frequency

CASE	CPU frequency (MHz)	Accelerator frequency (frames/sec)	System performance (frames/sec)	System power (mWatts)
CPU only	80 MHz	N/A	Baseline	Baseline
CPU + 5 hardware accelerators	1 MHz	1 MHz	5X	0.2X
CPU + 5 hardware accelerators	80 MHz	1 MHz	6X	0.5X

*Where baseline system performance = 0.164 frames/sec
*Where baseline system power = 102 mW



通过C2H降低系统功耗



硬件加速使您能够

- 满足性能要求
- 降低时钟频率
- 降低系统功耗

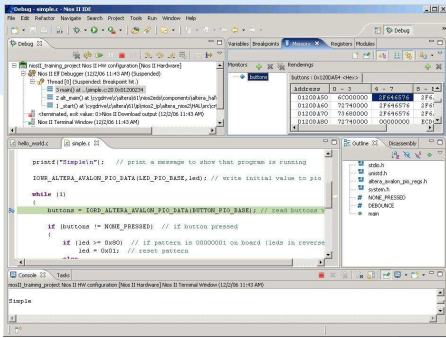




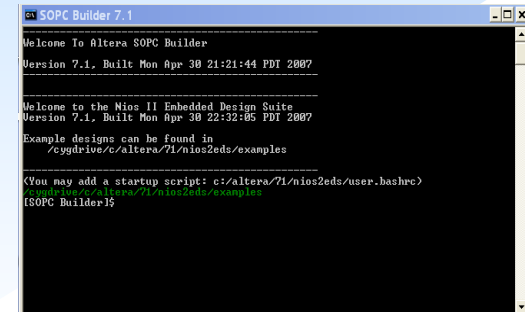
资源

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Nios II嵌入式设计包



Nios II IDE: 集成软件开发管理, 构建, 调试



Nios II软件构建流程: 通过构建实现快速编译, 脚本, 全面控制



嵌入式设计包



外设驱动器和运行时间软件库



Nios II嵌入式设计包

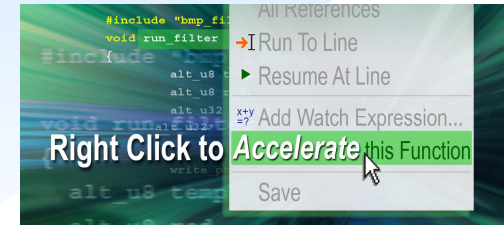
Micrium



*Micrium的实时操作系统**



*Interniche的商用级网络堆栈**



*C语言至硬件(C2H)编译器**



嵌入式设计包



LAUTERBACH



First Silicon Solutions

*FS2和Lauterbach的高级调试工具**

* 通过套件或者网络下载可进行全面评估试用——许可单独销售

NEEK设计实例

设计实例	汽车	航空电子	消费类	DSP	图形加速	GUI工具	现场更新	启动会话
Altera Application Selector							■	■
Altera Picture Viewer (VGA)			■					
Altia HMI (Blue, Red)	■				■	■		
Graphics Equalizer				■				
Imagem 2D Graphics					■			
Imagem aPhone			■		■			
Imagem Avionics		■			■			
Imagem Instrumentation	■				■			
Imagem Taquin					■			
Imagem Watch					■			

NEEK设计实例

设计实例	汽车	航空电子	消费类	DSP	图形加速	GUI具	现场更新	启动会话
MenuDemo PlanetWeb						■		
Micrium uC-GUI Demo						■		
PlanetWeb Photo Frame			■			■		
SLS uCLinux						■		
PlanetWeb SpectraWorks						■		
TES 2D D/AVE 2D Graphics					■			■
UNEEK Presenter								■
Mandelbrot C2H (VGA)								■
Spinning Cube (VGA)								



谢谢

ALTERA®