Freescale Technology Forum

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Cellular Platform Power Saving Techniques

PM106

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eXtreme Energy Conservation Topics

- RF Circuits
  - **Low voltage RF CMOS – impact of power system architecture**

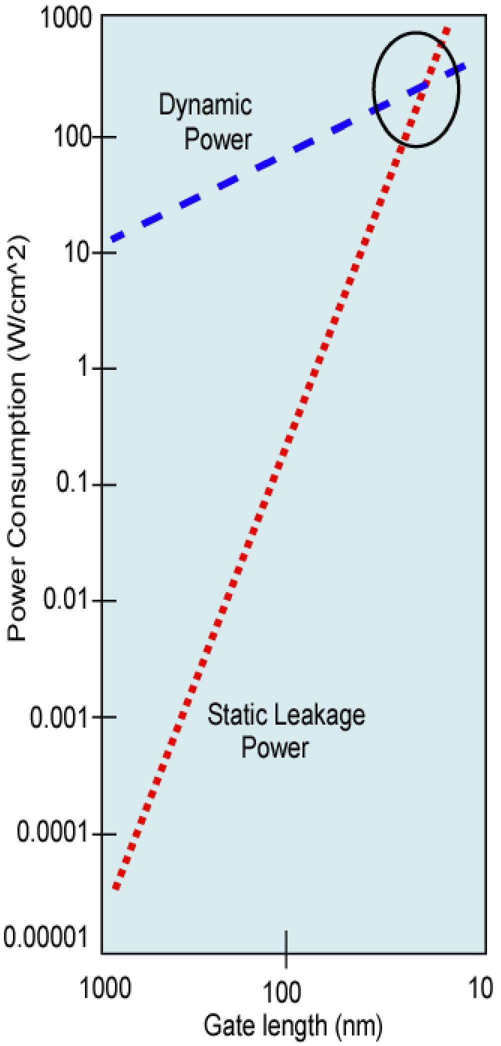
- Baseband – **power management techniques**
  - **Dynamic process temperature compensation (DPTC)** dynamically adjusts the supply voltage relative to the current temperature and the manufacturing process used
  - **Dynamic voltage frequency scaling (DVFS)** reduces operating voltage to the minimum level needed to support only the minimum operating frequency required by applications at any given moment
  - **Active well biasing** reduces standby leakage by lowering the well voltage of the transistor
  - **Technology choice** for optimum trade-offs between speed and low-power, high-performance, but with leaky transistors (low voltage threshold) versus ultra-low power semiconductor circuits (high voltage threshold) for functional modules with modest performance requirements.

►Power Management IC

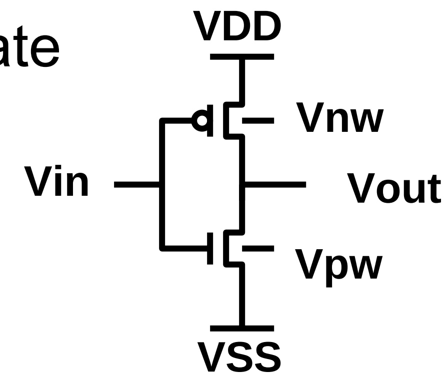
- **Smart MOS Process**
  - low cost CMOS process
- **Voltage conversion**
  - Efficient switching regulators
  - Standby controls for low power states
  - Support for DVFS and DPTC control

CMOS transistor leakage versus process geometry

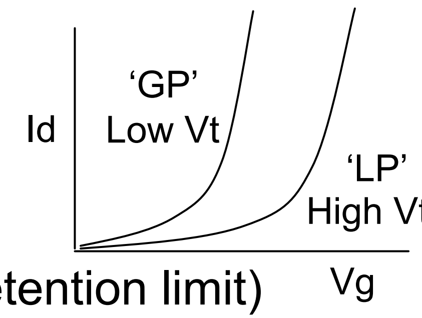
- Leakage becomes a significant issue at 90 nm process and smaller
- Below 32 nm leakage approaches active power
  - (active power -> CV^2F)
  - (static leakage power -> non-clocked power)
    - 90 nm : 15pA/um
    - 65 nm : 20pA/um
    - 45 nm : 250pA/um
    - 32 nm : 450pA/um
- Gate oxide thickness proportional to process geometry node
  - Leakage and maximum supply voltage



CMOS Leakage



- ▶ **Leakage** is a linear function of width to length of gate
- ▶ **Leakage** is exponential with temperature
  - Idss ~ 0.194 * exp(- 6155.6 / T),
    T in Kelvin (LPc90 @ 1.0 vdc Vdd)
  - About 50x from 27 deg C to 100 deg C (die temp)



- ▶ **Leakage** is slightly exponential with supply voltage
  - Gate oxide thickness limits maximum Vdd
  - Speed greater for greater Vdd (greater gate drive / gm)
  - Lowering supply Vdd reduces static leakage (register retention limit)
- ▶ **Leakage** is logarithmic to gate threshold (GP vs. LP process)
  - Approximately 85 mVdc drop in gate threshold increases leakage 10x
  - Raising gate-source Vt (better turn off) degrades speed performance
  - Process can be set to higher speed performance or lower leakage

eXtreme Energy Conservation on Cellular Baseband

- **Dynamic process temperature compensation (DPTC)**
  - Dynamically adjusts the supply voltage relative to the temperature and the manufacturing process used
    - **Factory set implementation**
      - Fuses are set to indicate best Vdd for desired clock speed
        - Read by software to set power management Vdd setting
    - **Real time DPTC**
      - Software controls Vdd based on reference circuits on die

- **Dynamic voltage frequency scaling (DVFS)**
  - Reduces Vdd to the minimum level needed to support operating frequency required by applications at any given moment
  - Requires finite amount of time to change settings
    - Power management controlled voltage slew
    - Clock setting decrease or increase must follow voltage change to ensure sufficient Vdd to support clocking rate

- **Bulk bias change**
  - Negative channel isolation well bias voltage raises Vt slightly
  - Positive effect diminished below 90 nm process nodes

eXtreme Energy Conservation on Cellular Baseband

▸ Save and Restore

- Prior to entering deep sleep, software saves critical register/memory
- Vdd is shut down to circuit sections that were backed up
- Software retrieves and restores register setting upon reactivation

▸ State retention power gating (SRPG)

- Prior to entering wait or deep sleep, critical registers of high performance (high leakage) circuits are automatically backed up to parallel low leakage registers
- Vdd is shut down to high leakage circuits while low leakage backup registers Vdd is maintained
- Usually restricted to processor core registers and other critical registers due to die area impact. (no large memory blocks)

▸ Clock gating

- Inactive circuit blocks are ‘frozen’ by shutting down their clocking

Power Mode Definitions for MXC91321 Cellular Baseband

Mode	DSP/MCU	Peripherals	Ref Clk	PLL	Regulator
RUN High	Active	Some Active	On	On	Elevated Voltage
RUN Low	Active	Some Active	On	On	Nominal Voltage
WAIT/DOZE	Disabled	Some Active	On	On	Nominal Voltage
STOP	Disabled	Disabled	On	Off	Nominal Voltage
SLEEP	Disabled	Disabled	Off	Off	Reduced Voltage

Power Mode Definitions for MXC91321 Cellular Baseband

Domain	Logical Partition	Nominal Voltage	Maximum Frequency	Notes
BP Domain	P2002 Core	1.6V	312MHz	Overdrive mode
		1.2V	208MHz	
		1.0V	32.768kHz	Reduced V, Leakage control activated
	BP AHB Bus Clock	1.6V	125MHz	
		1.2V	104MHz	
		1.0V	32.768kHz	Reduced Voltage
	BP IP Bus Clock	1.6V	62.5MHz	
		1.2V	52MHz	
		1.0V	32.768kHz	Reduced Voltage
AP/COM Domain	ARM1136™ Core	1.6V	532MHz	Overdrive mode
		12V	400MHz	
		1.0V	32.768kHz	Reduced V, Leakage control activated
	AP/COM AHB Bus Clock	1.2V / 1.6V	133MHz	
		1.0V	32.768kHz	Reduced Voltage
	AP/COM IP Bus Clock	1.2V / 1.6V	66.5MHz	
		1.0V	32.768kHz	Reduced Voltage

65 nm Power Saving Modes

Mode	Apps Proc	DSP	Gen Logic/ Accelerators
Ultra-High Performance	**1.1V** 1000MHz	**1.2V** 400MHz	**1.2V** 133MHz
High Performance	**1.0V** 800MHz	**1.2V** 400MHz	**1.2V** 133MHz
Medium Performance	**1.0V** 800MHz	**1.0V** 200MHz	**1.2V** 133MHz
Low Performance	**0.8V** 200MHz	**1.0V** 200MHz	**1.2V** 133MHz
Ultra-Low Performance	**0.8V** 200MHz	**1.0V** 200MHz	**1.0V** 66.5MHz
Standby (DSM)	**0.75V**	**0.9V**	**0.9V**

65 nM Use Case driven DVFS Modes

Mode	Apps Proc	DSP	Gen. Logic	Video Call	Video Record	Video Play	MP3	HSDPA/ E.EDGE	EDGE	2G/3G Voice	2G/3G Standby
UHPM	**1.1V** 1000MHz	**1.2V** 400MHz	**1.2V** 133MHz								
HPM	**1.0V** 800MHz	**1.2V** 400MHz	**1.2V** 133MHz								
MPM	**1.0V** 800MHz	**1.0V** 200MHz	**1.2V** 133MHz								
LPM	**0.8V** 200MHz	**1.0V** 200MHz	**1.2V** 133MHz								
ULPM	**0.8V** 200MHz	**1.0V** 200MHz	**1.0V** 66.5MHz								
Standby (DSM)	**0.75V**	**0.9V**	**0.9V**								

RF power savings

- RF CMOS
  - Operating Vdd 1.0 to 1.4 vdc
    - Advantage to power converters (switching) supply from battery.

- Interfaces
  - Low voltage, differential digital (LVDS) signaling
    - Pushing large signal swings at higher and higher frequencies is not power efficient and creates EMI noise

- RF power amplifiers
  - Power converters (switchers)
  - Stage by-passing

Power Management Integrated Circuit Power Techniques

- Why we still have PMIC chips
  - Handle supply voltage of battery and charging circuitry
  - Cost effective – less process layers
- SMOS10 -> power management, 130 nm low cost process
  - Up to 20 volts capable
- Higher speed voltage converter switching for smaller external components – higher switching speed = smaller L & C of filter
  - Challenging drive power (CV^2F) of switching transistor gates
    - Pulse skipping modes for low load demands
    - Change to linear mode at very low load demands
- System interlocking control
  - Continuous feedback DVFS, voltage <-> clocking speed

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Software involvement in Power reduction

- Deep Sleep Mode
  - Architect early in software plan
- DVFS utilization
  - Resource loading management – clock speed & Vdd set based on need
- Modem Processor SW
  - Batch use of interrupts where possible
    - Consideration for cache integrity
  - L1 cache/RAM/ROM fastest
    - Create less clock cycle waits for L2 or external memory
    - ROM much less capacitive load on processor bus due to smaller cell size
      - Total loading on processor bus limits processor speed and impacts power consumption
- Applications Processor SW
  - Power management Driver
    - Efficient OS 'tick' utilization, batching where possible

Related Session Resources

Session Location – Online Literature Library

http://www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=052577903644CB

Sessions

Session ID	*Title*

Demos

Pedestal ID	*Demo Title*

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